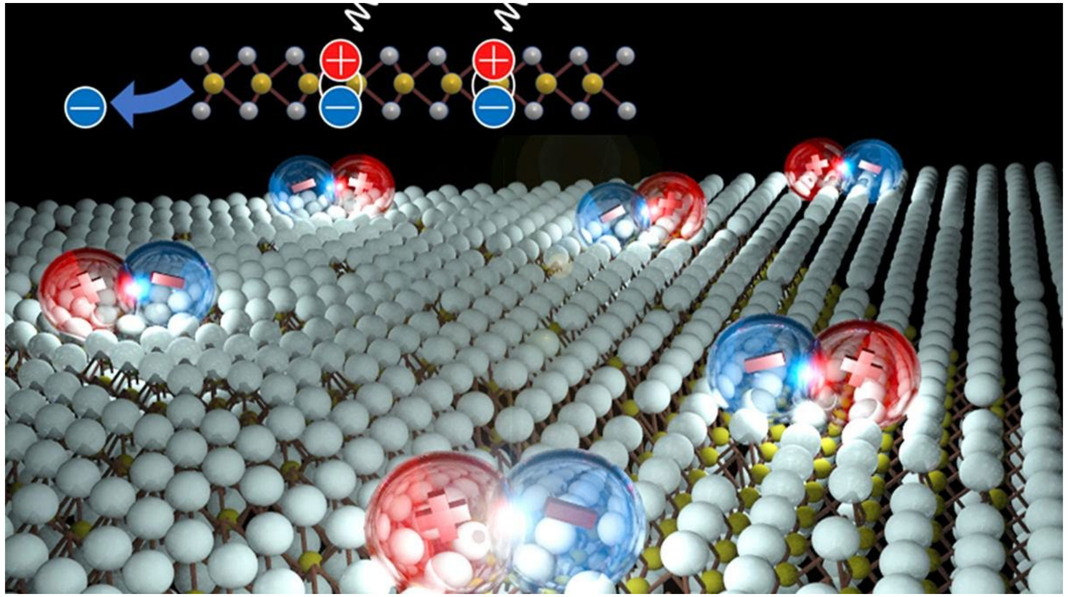
Harvard John A. Paulson
School of Engineering
and Applied Sciences

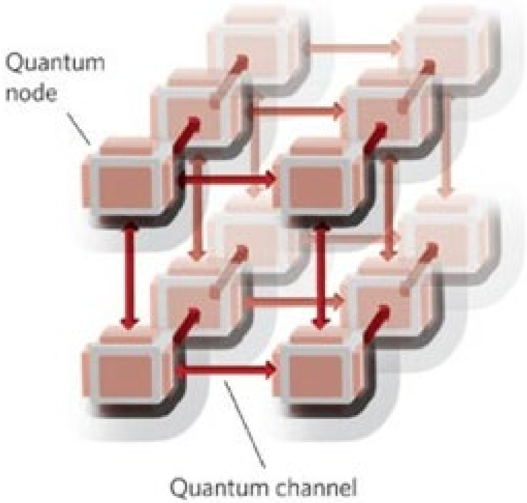
Department of Chemistry and Chemical Biology
Harvard

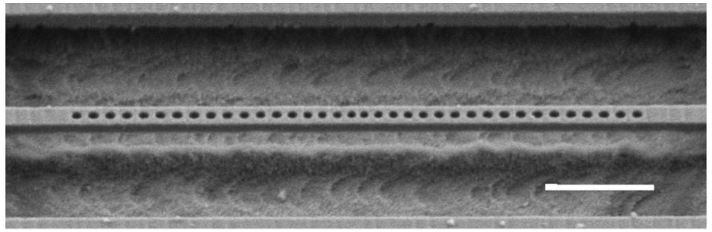
From Sand to Transistor: Microfabrication in a Day

Joy Cho, Matt Yeh – Saturday, November 14th, 2020

About Me – Matt







Kimble, H.J., *Nature* 453.7198 (2008).
Bracher, D.O., et al., *PNAS 114.16 (2017).*

About Me – Joy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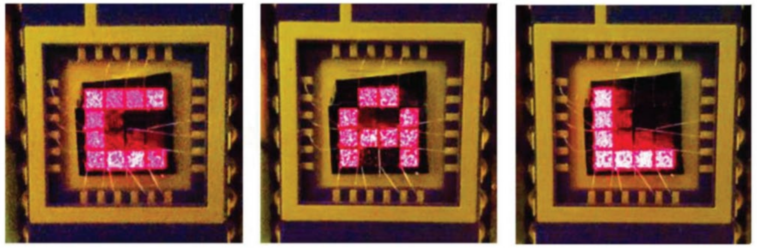
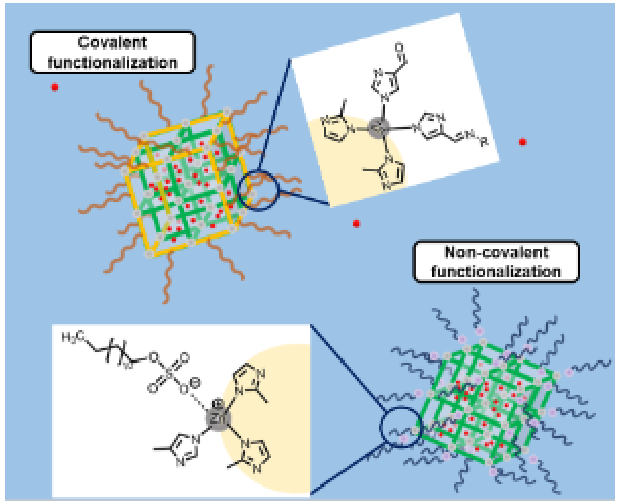


DEPARTMENT OF CHEMISTRY AND CHEMICAL BIOLOGY



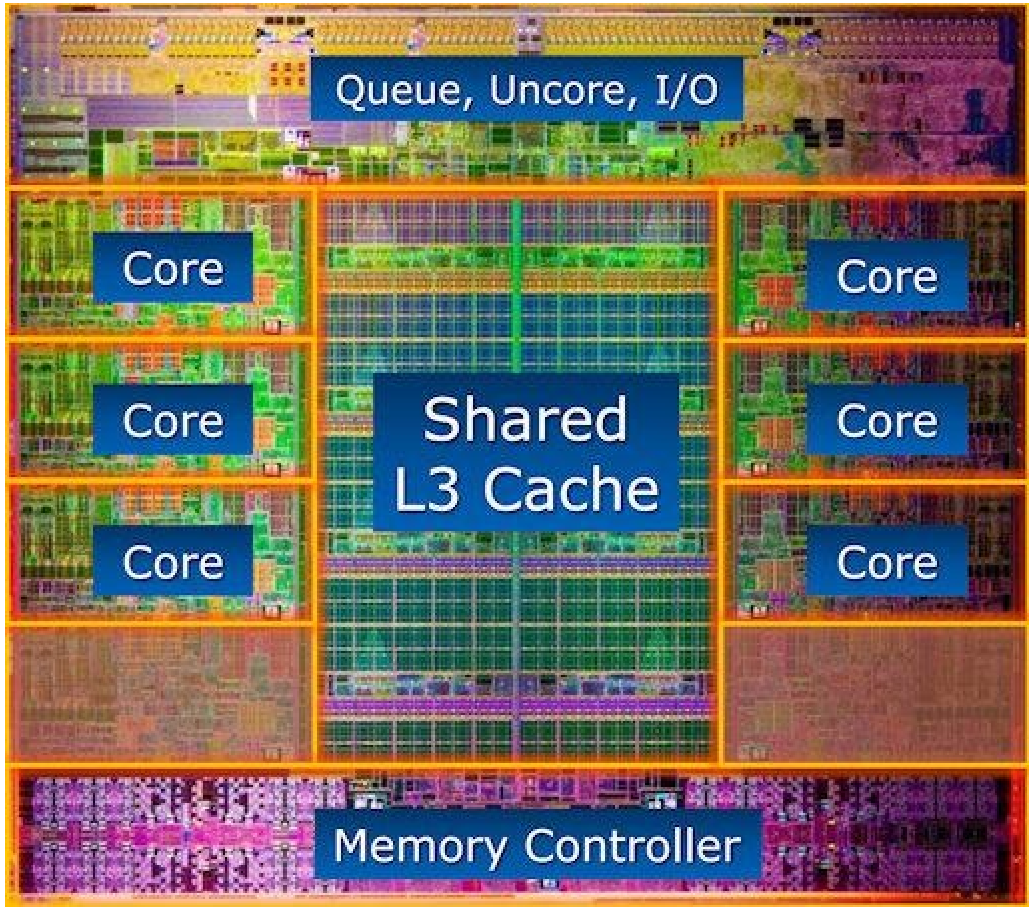
Tell us about yourself!

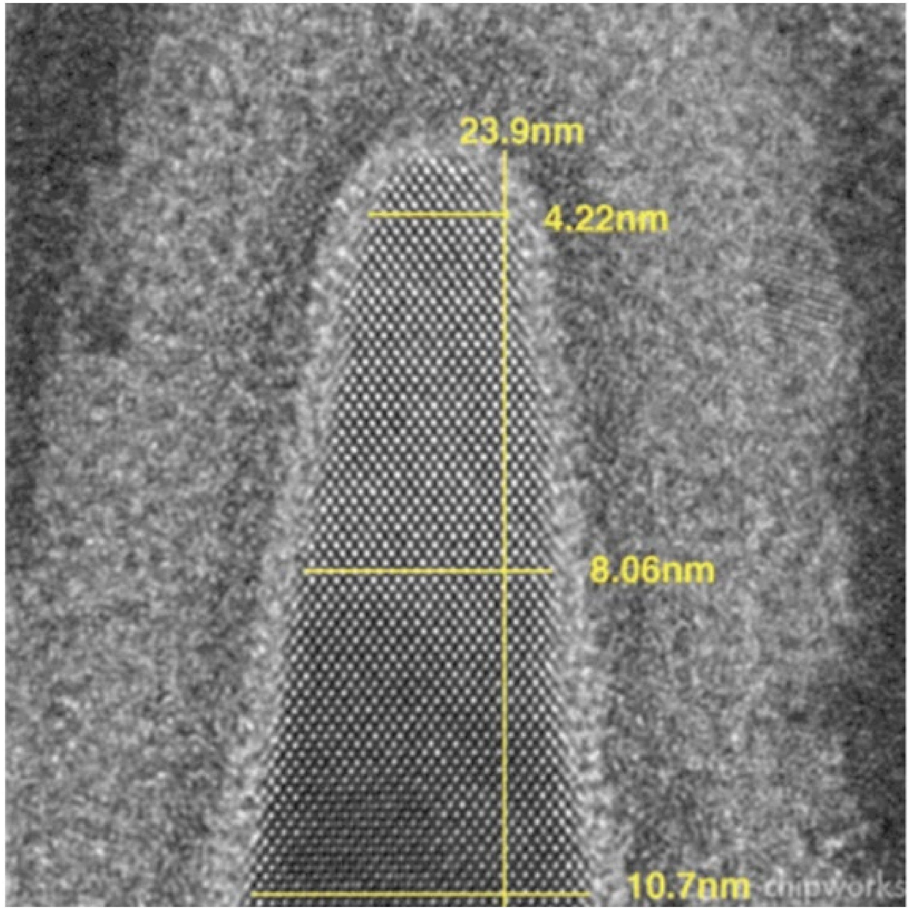
- Name
- Something interesting you learned recently, or something you want to learn about!

The Axolotl Song:
https://www.youtube.com/watch?v=MxA0QVGVEJw

How do we get from here…

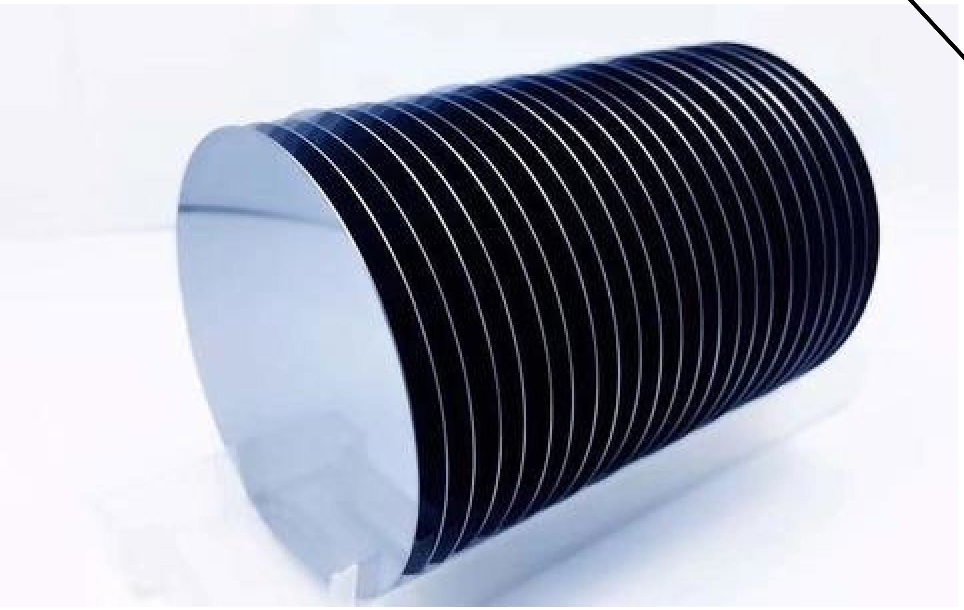
…to here?

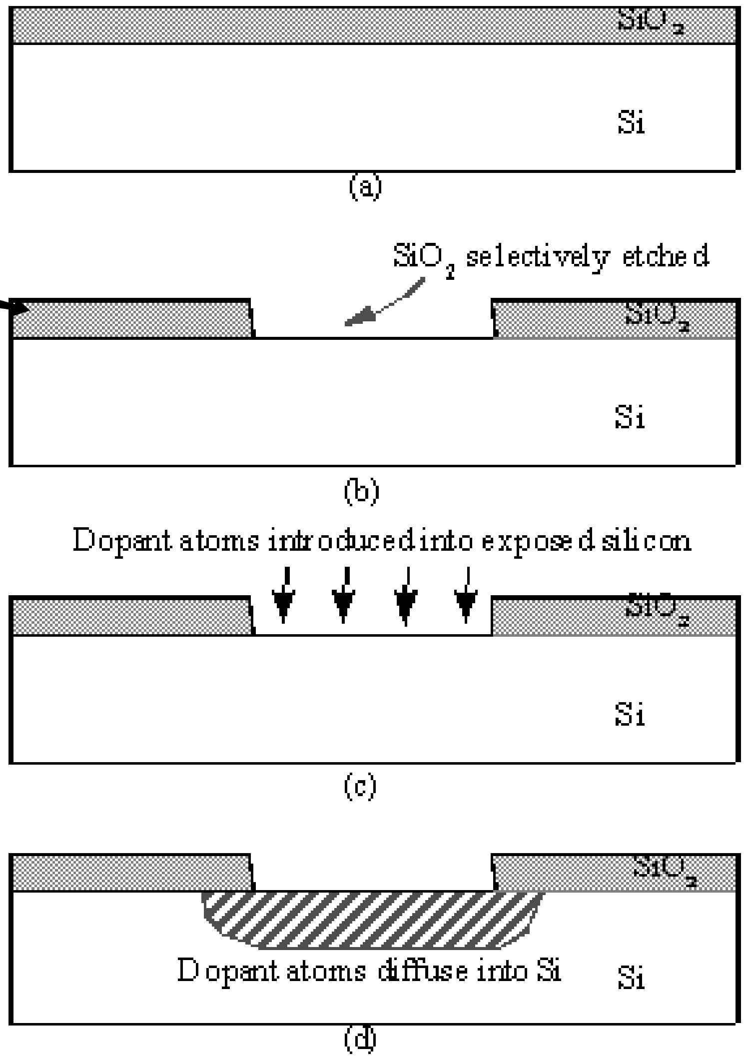

Queue, Uncore, I/O
Core
Core
Core
Shared L3 Cache
Core
Core
Core
Memory Controller


23.9nm
4.22nm
8.06nm
10.7nm
chipworks

Essential Steps of Microelectronic Fabrication

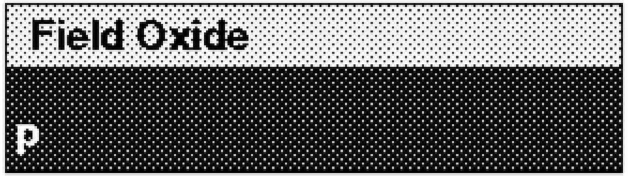
1. Deposition/growth of material
2. Patterning of material
3. Removal (etching) of material
4. “Doping” of material





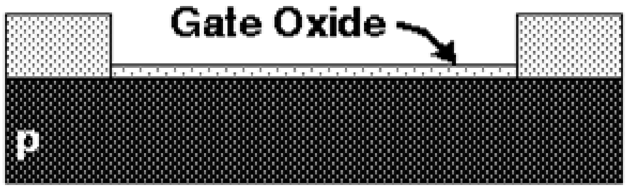
Example Process

Week 2: Field Oxidation - 5200 A

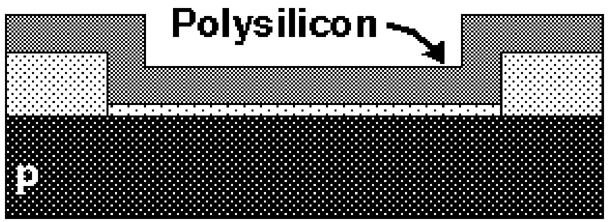


Week 3: Active Area Photolithography

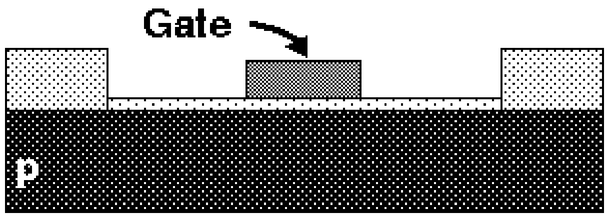
Week 4: Gate Oxidation - 800 A



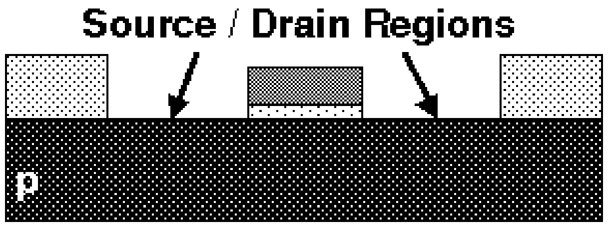
Week 5: Poly-Si Deposition

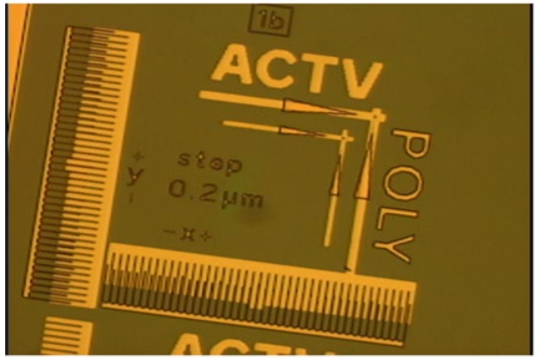


Week 6: Gate Photolithography



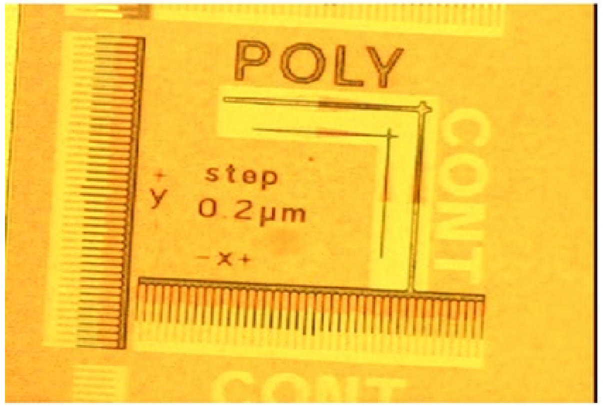
Week 6: Clear Source and Drain



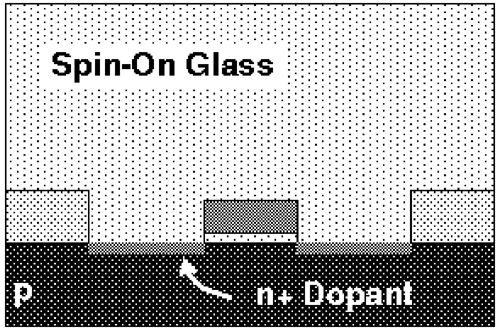


Based on EE143 slides from A. Javey

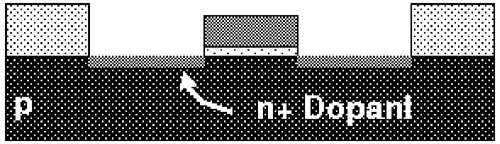
Example Process (cont.)



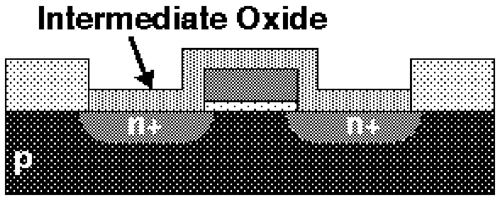
Week 7a: Source-Drain Deposition (N+)



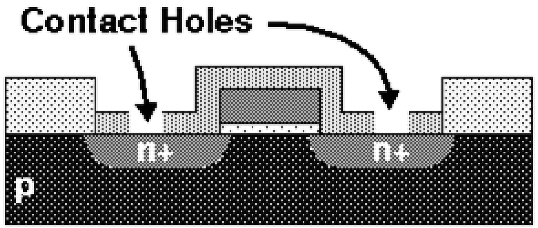
Week 7b: Spin-on Glass Strip



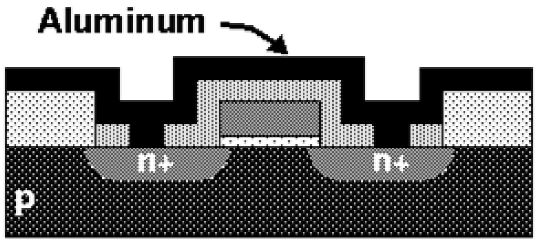
Week 7b: Drive-In Oxidation



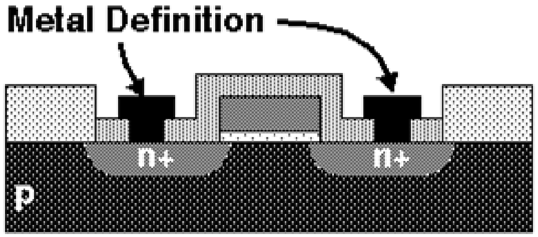
Week 8: Contact-Hole Cut (Mask #3 - CONT)

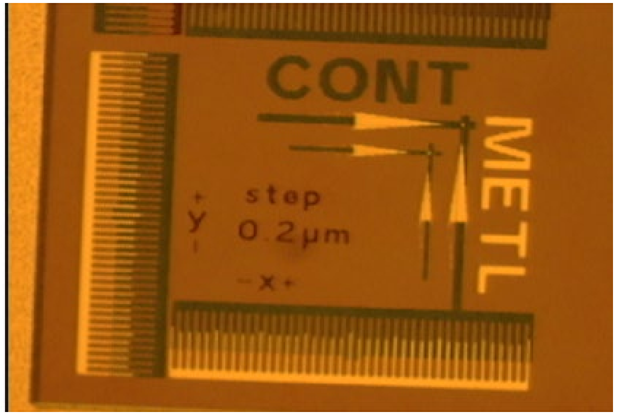


Week 9: Metallization



Week 10: Metal Definition

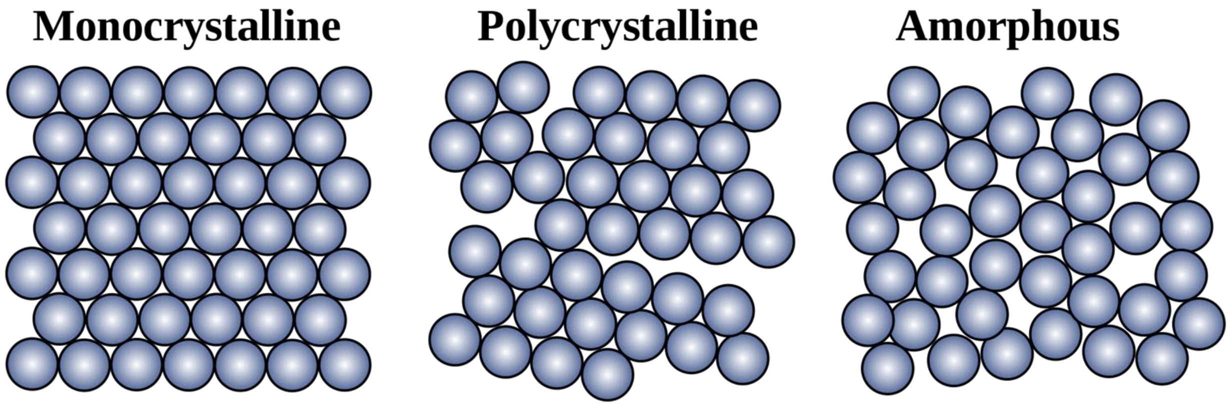




Based on EE143 slides from A. Javey

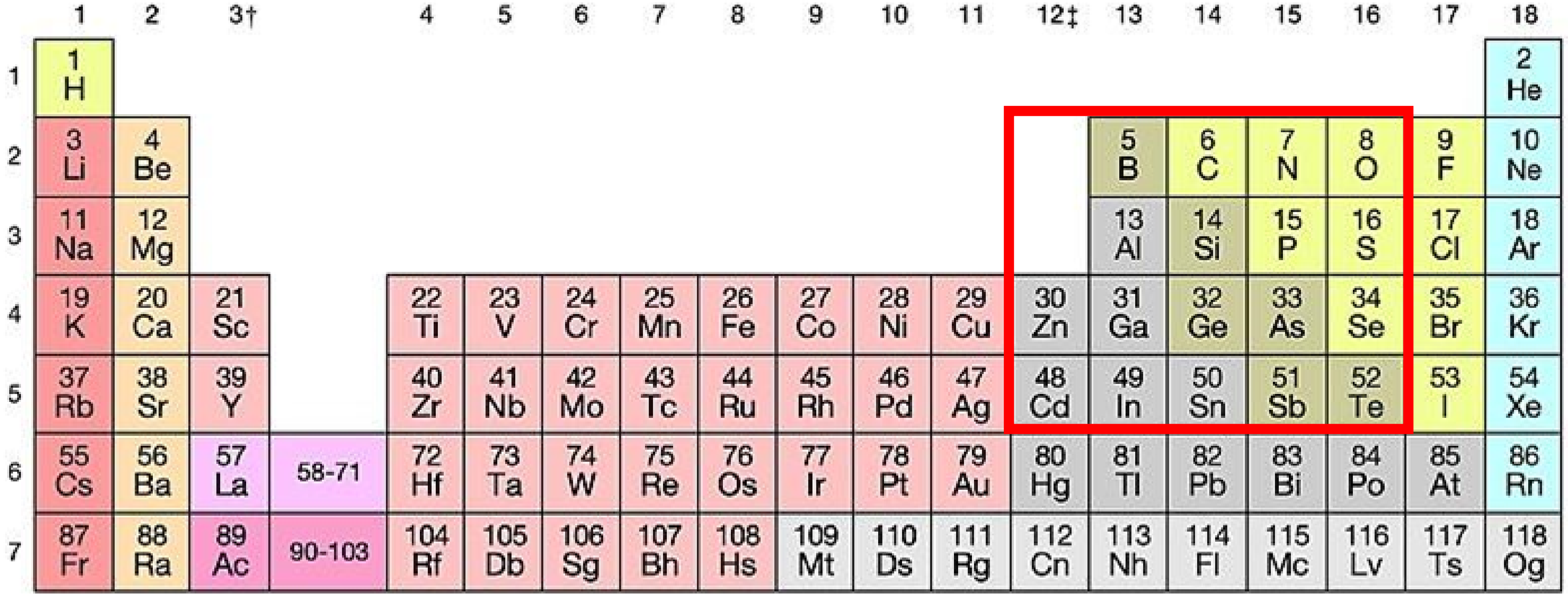
Introduction to Materials

- Conductors
  - Low resistivity $(10^{-6} < \rho < 10^{-5}\ \Omega\,\mathrm{cm})$
  - Example: metals
- Insulators
  - High resistivity $(10^{14} < \rho < 10^{15}\ \Omega\,\mathrm{cm})$
  - Example: SiO_2 ("oxide"), Si_3N_4 ("nitride")



- Semiconductors
  - Somewhere in between conductors and insulators
  - Typically crystalline, although using polycrystalline and amorphous semiconductors in devices in an ongoing area of research!
  - Q: Why do you think people are trying to do this?

Semiconductors and the Periodic Table



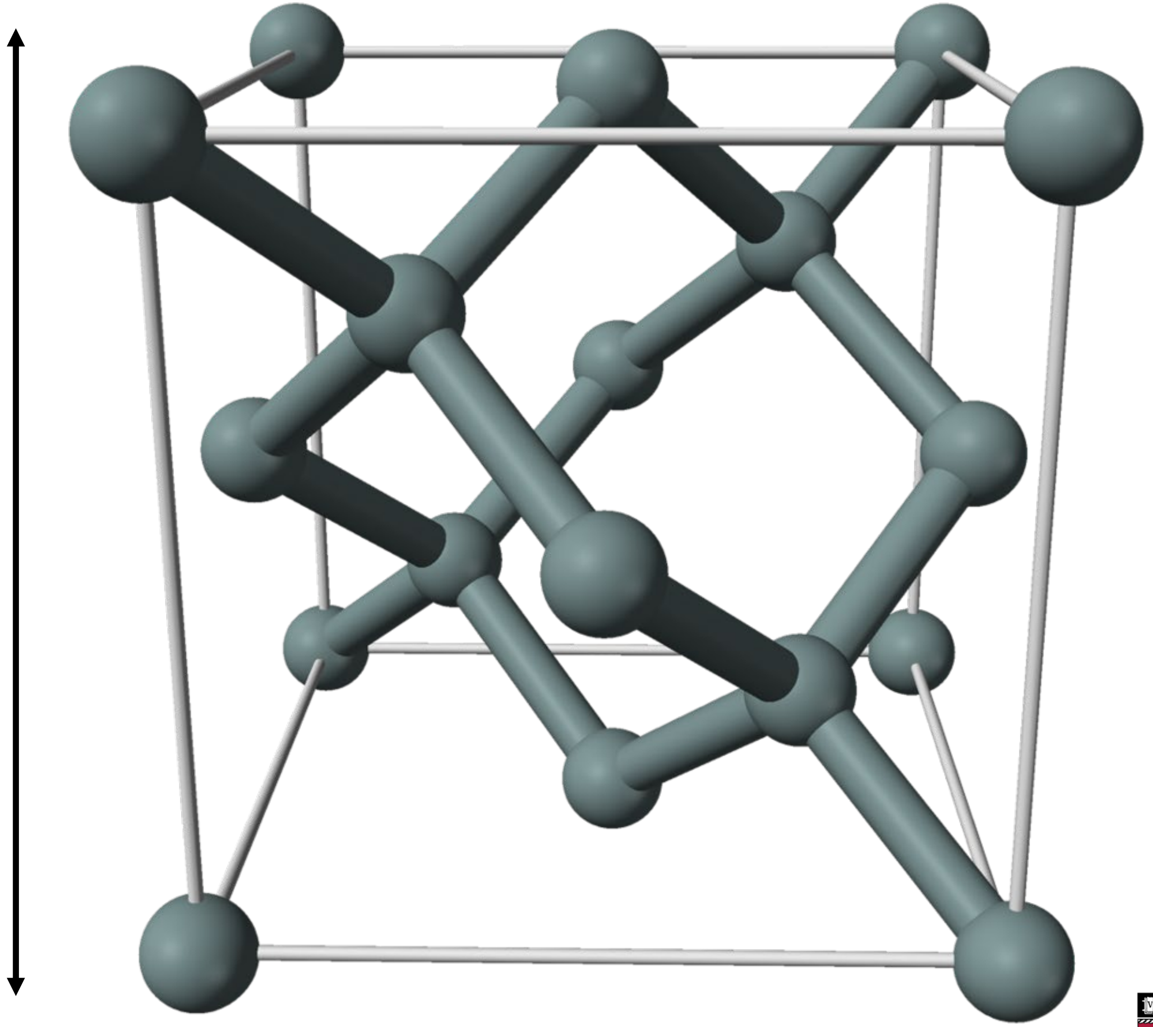
	1	2	3†		4	5	6	7	8	9	10	11	12‡	13	14	15	16	17	18
1	1 H																		2 He
2	3 Li	4 Be												5 B	6 C	7 N	8 O	9 F	10 Ne
3	11 Na	12 Mg												13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
4	19 K	20 Ca	21 Sc		22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
5	37 Rb	38 Sr	39 Y		40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
6	55 Cs	56 Ba	57 La	58-71	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
7	87 Fr	88 Ra	89 Ac	90-103	104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Cn	113 Nh	114 Fl	115 Mc	116 Lv	117 Ts	118 Og

- Elemental: C, Si, Ge
- Binary: SiC, GaAs, InP
- Ternary: AlGaAs, InGaAs

Notice any trends?

Silicon Crystal Structure

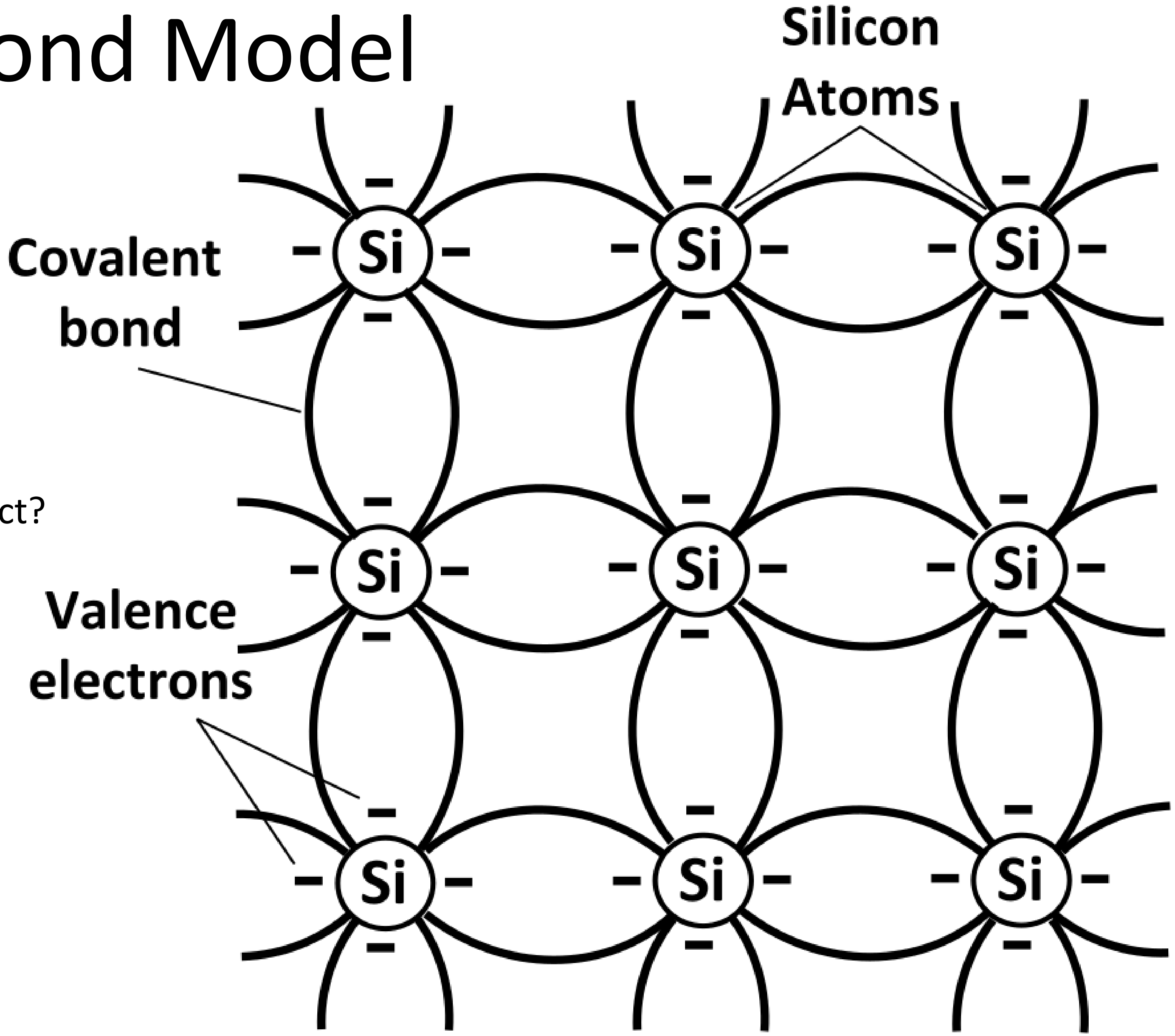
- “Diamond cubic” lattice structure
- Each atom has 4 nearest neighbors



Lattice constant (a) = 0.543 nm

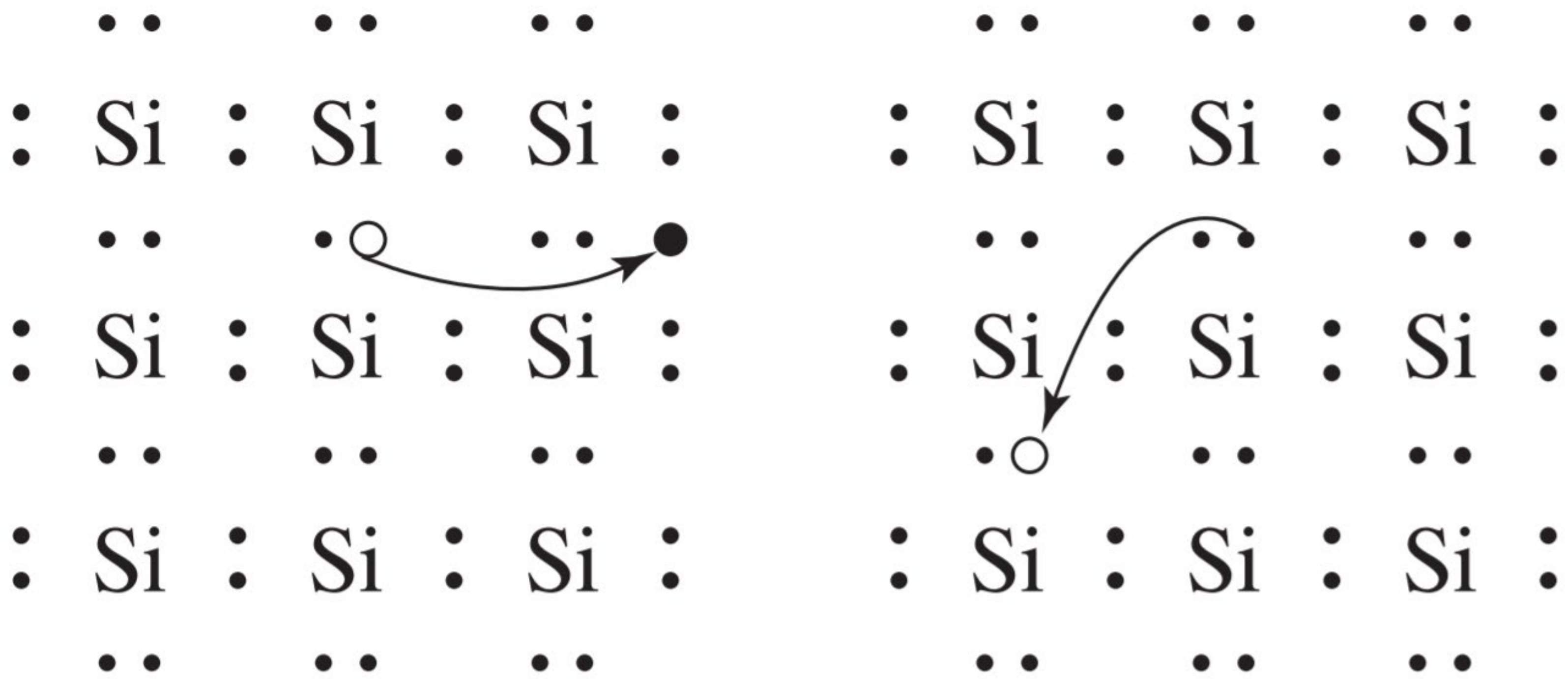
Silicon Bond Model

If this was how silicon looked, would it conduct?



Bond Model of Electrons and Holes

- When an electron breaks away from the bond and becomes a *conduction electron*, a *hole* is also formed.

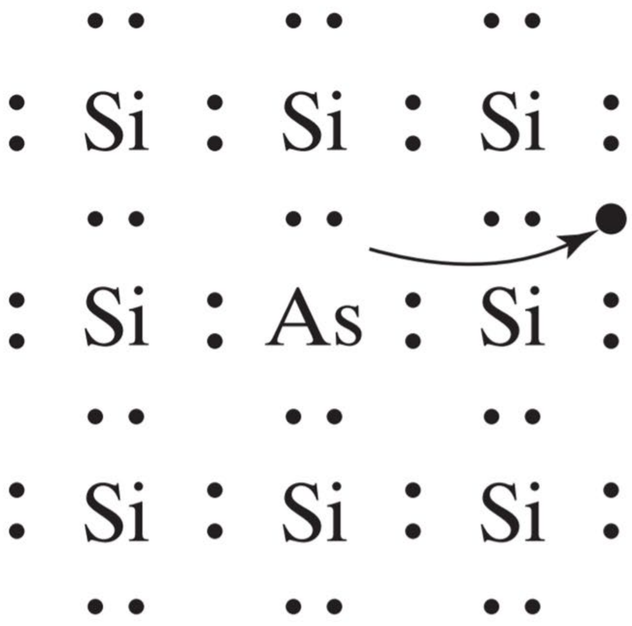


Holes

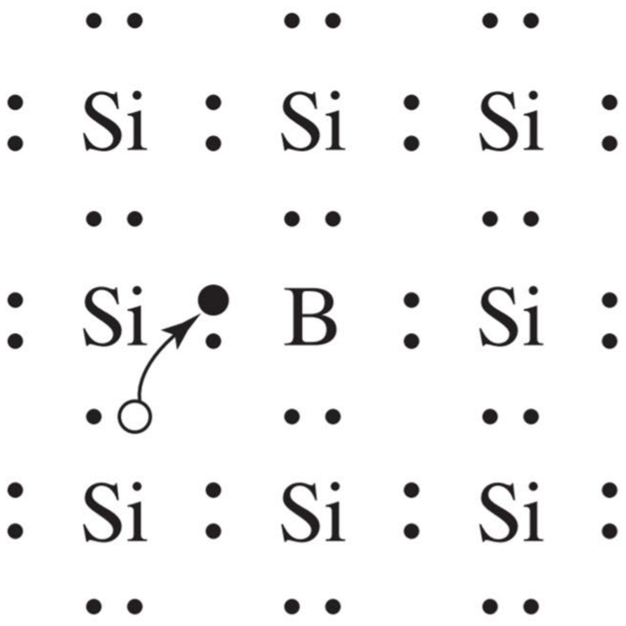
- A hole is a mobile positive charge associated with a half-filled covalent bond
- For the most part, we can treat it as a positively charged particle in a semiconductor, as real as an electron.

Doping

- Conduction electron concentration: n [cm^{-3}]
- Conduction hole concentration: p [cm^{-3}]
- Intrinsic carrier concentration: n_i
  - Without doping, $n=p=n_i$
- With doping, we can change the electron or hole concentration!



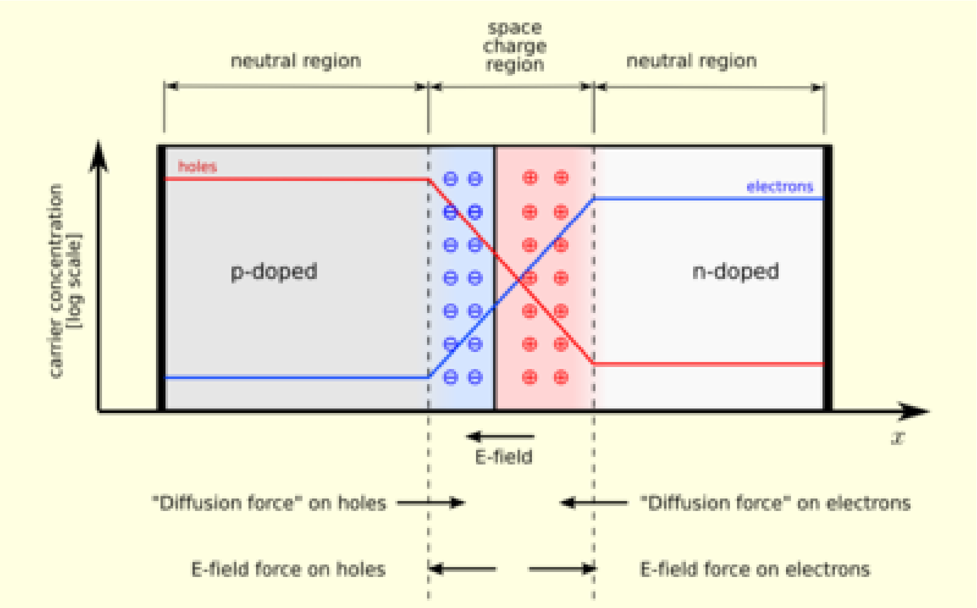
e.g. Arsenic in Silicon, an electron **donor**



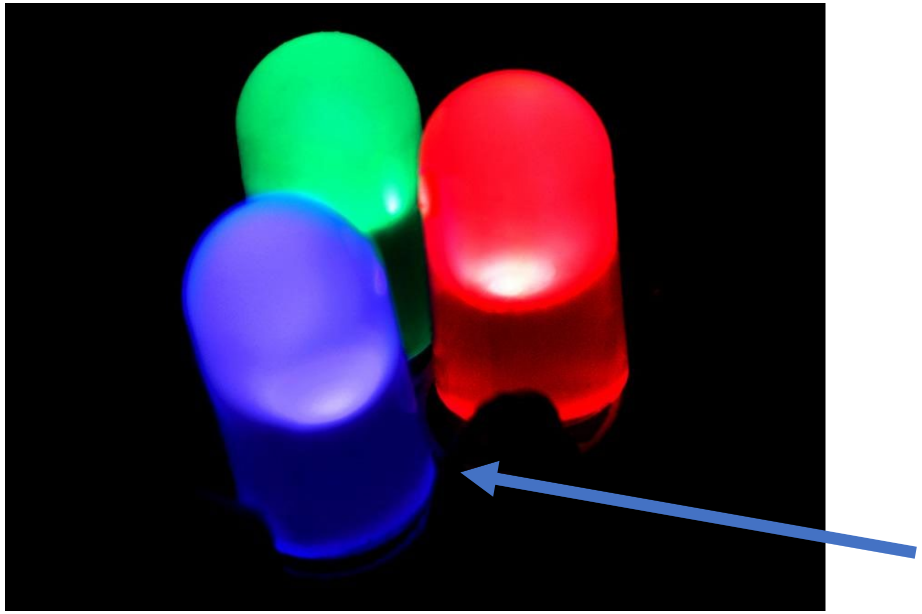
e.g. Boron in Silicon, an electron **acceptor** (adds a hole)

Why do we want doping?

"pn junction" forms basis of many modern devices!



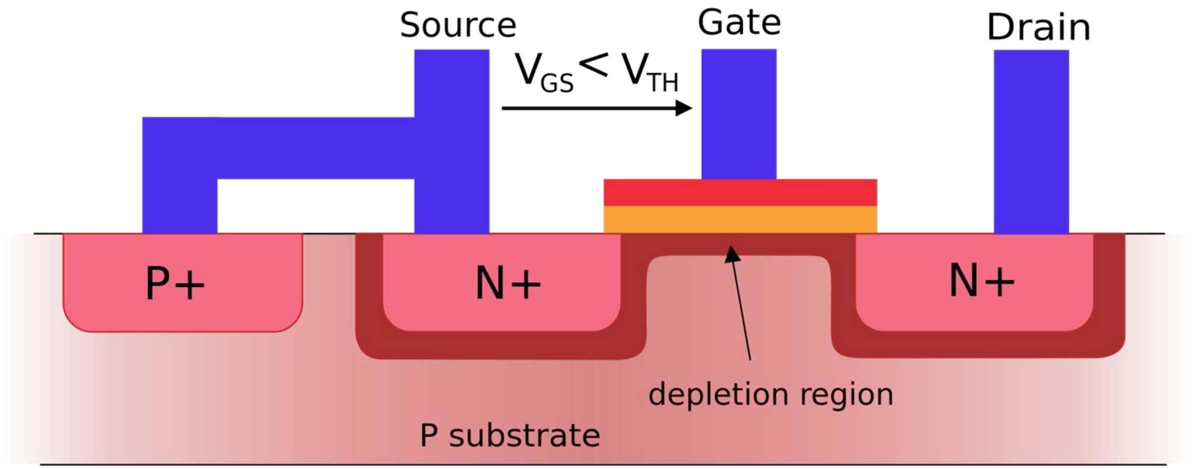
LED



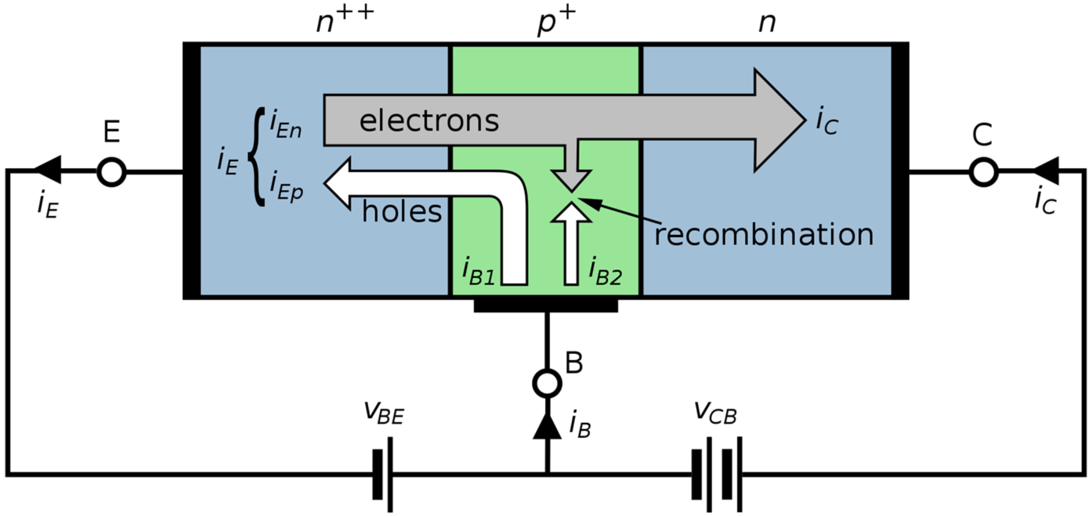
Nobel Prize!

Solar Cell

Why do we want doping?



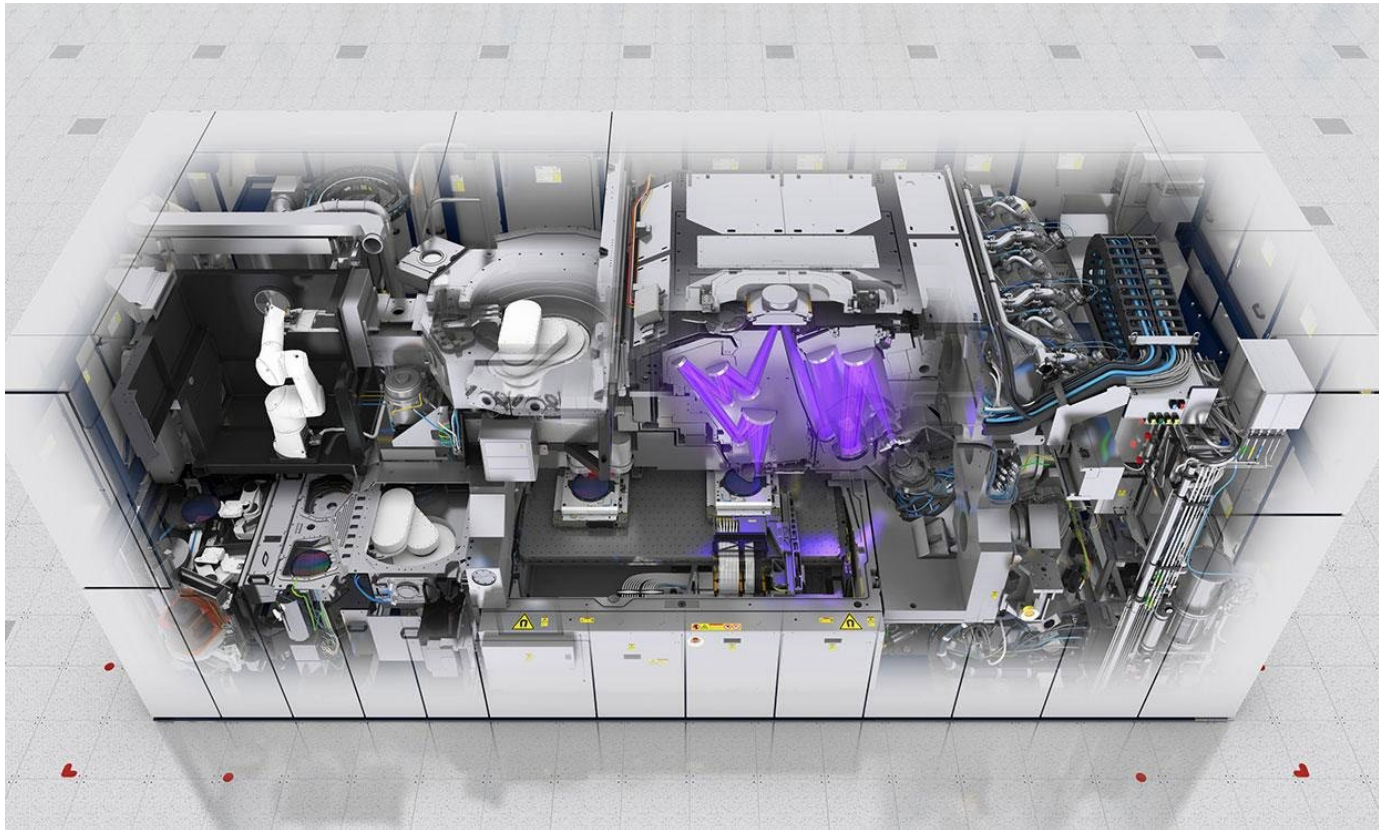
MOSFET
Metal Oxide Semiconductor
Field Effect Transistor



BJT
Bipolar Junction Transistor

Photolithography

- Greek: phos (light) + lithos (stone) + graphein (to write)

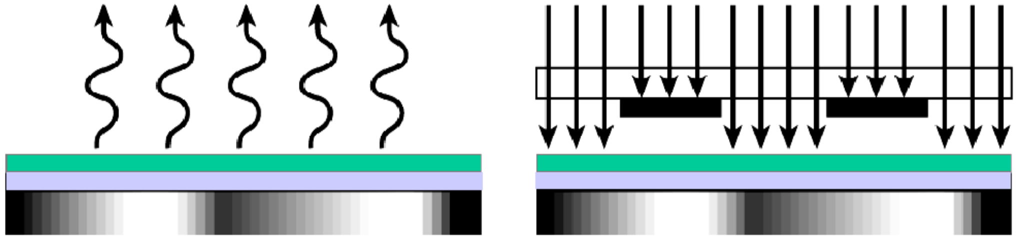


Next-generation EUV Lithography Tool: ASML

Photolithography Process

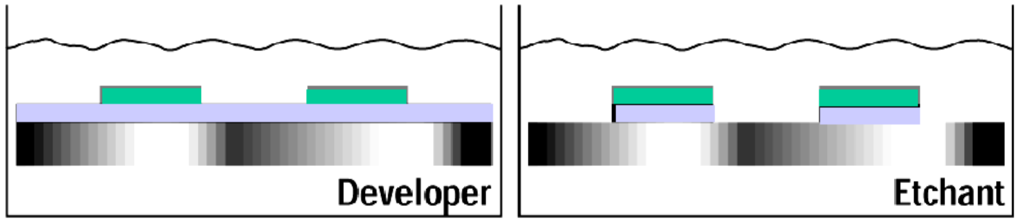
(1) Starting wafer with layer to be patterned

(2) Coat with photoresist



(3) Bake the resist to set its dissolution properties

(4) Expose resist by shining light through a photomask



(5) Immerse exposed wafer in developer

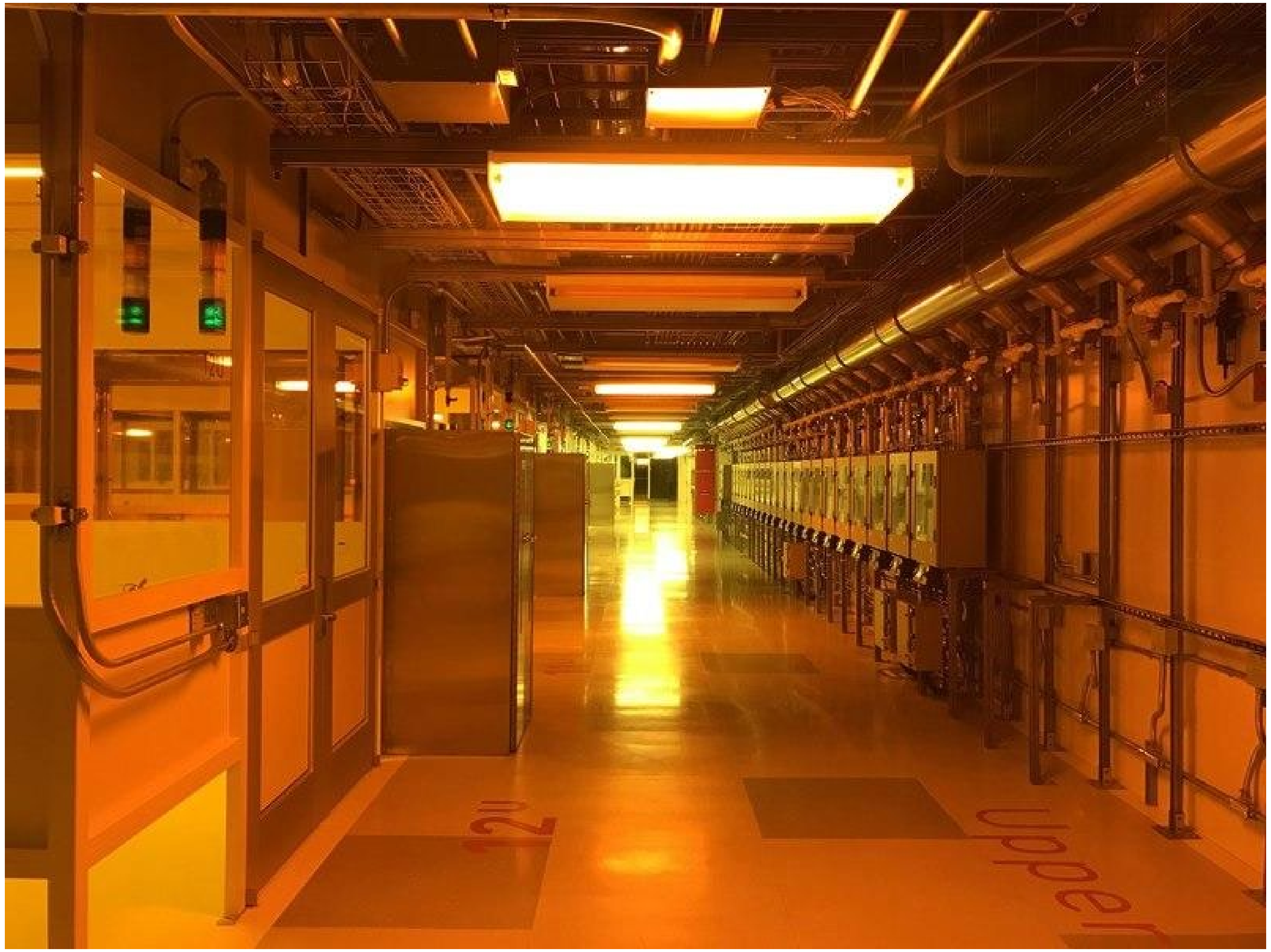
(6) Etch the film

- Dehydration bake
- Adhesion promoter application
- Resist application
- Softbake
- Exposure
- Post exposure bake*
- Develop cycle
- Hardbake
- Resist stabilization*

*Optional steps

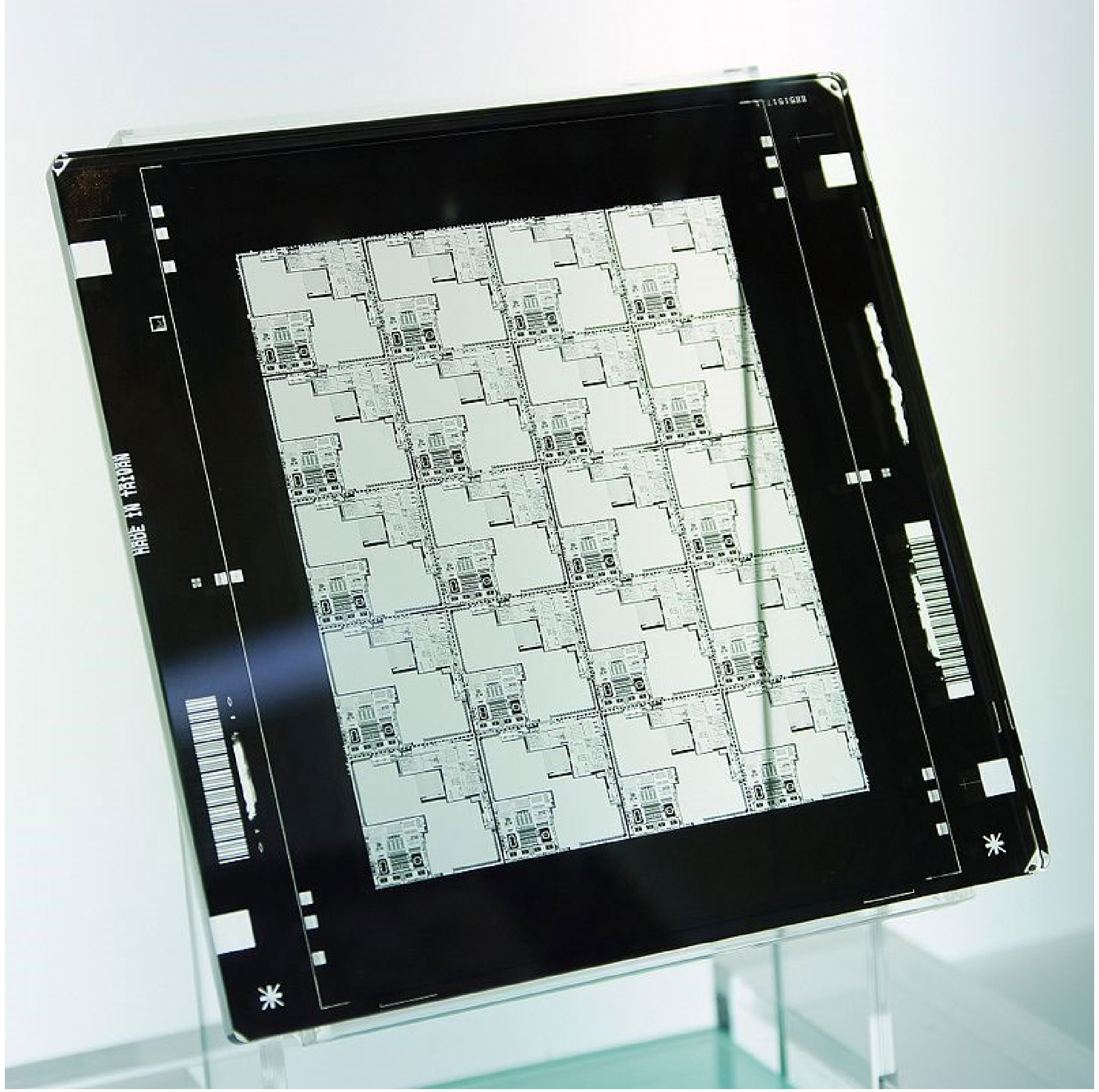
Based on EE143 slides from A. Javey

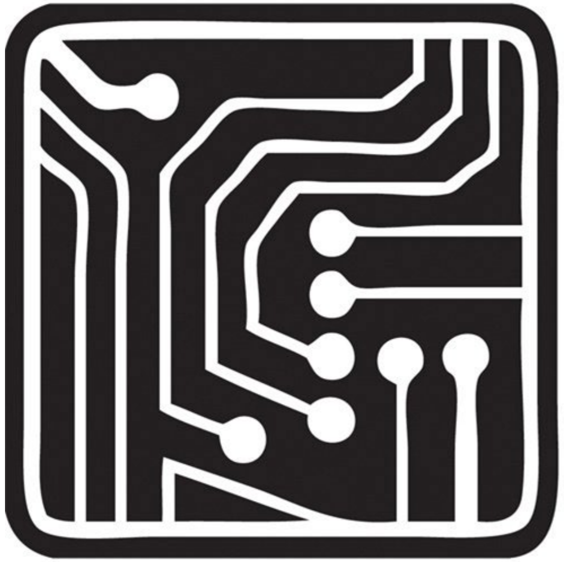
Why are cleanrooms yellow/orange?



New MIT Nano cleanroom

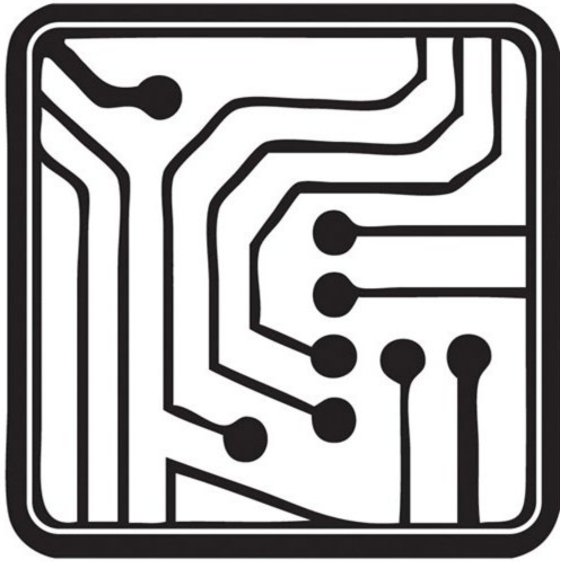
Photomasks





Dark Field Mask

What is drawn in CAD design gets exposed to light

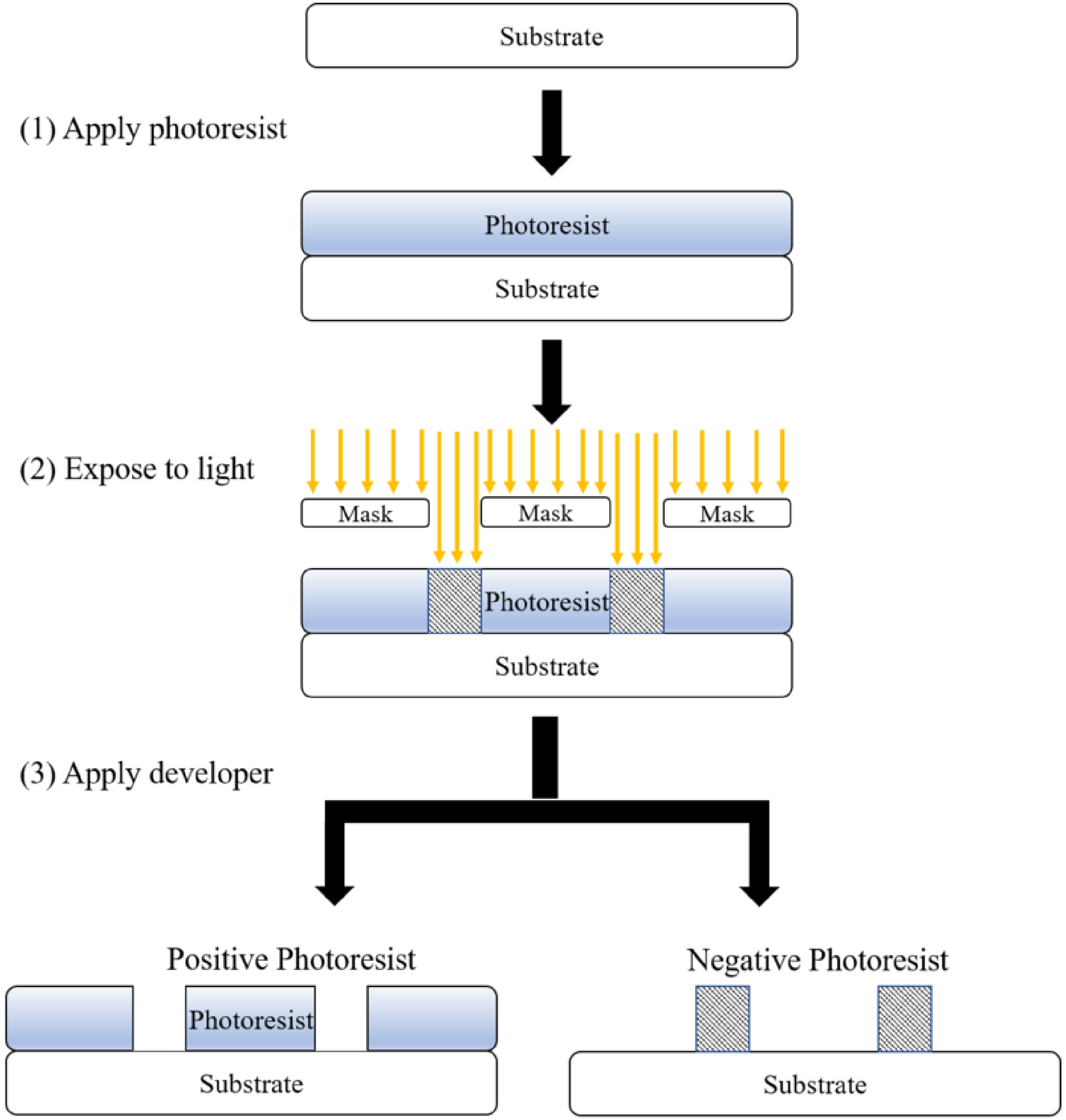


Clear Field Mask

What is drawn in CAD design blocks light

Photoresist—Two Types

- Negative Resist
  - Polymer (molecular weight ~65000)
  - Light sensitive additive promotes crosslinking between chains when activated: “strengthens resist”
- Positive Resist
  - Polymer (MW~5000)
  - Light sensitive additive (“dissolution inhibitor”) gets deactivated when exposed to light: “weakens resist”

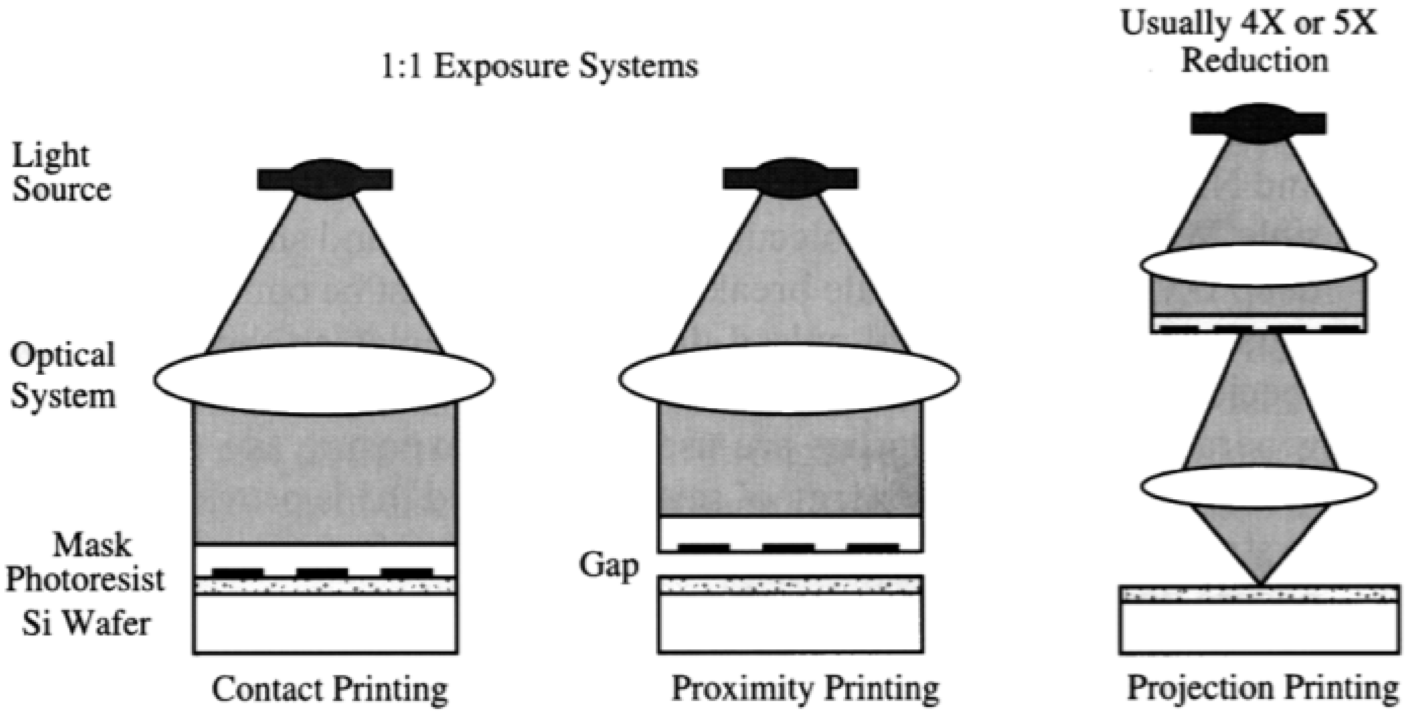


Pros/Cons of Positive/Negative Resists

- Negative Resist
  - More sensitive to light (less exposure dose needed to completely remove the film)
  - More resistant to chemicals—better as a chemical mask when etching
  - Cheaper
  - BUT, lower resolution (why?)
- Positive Resist
  - Higher resolution
  - BUT, less sensitive → lower throughput

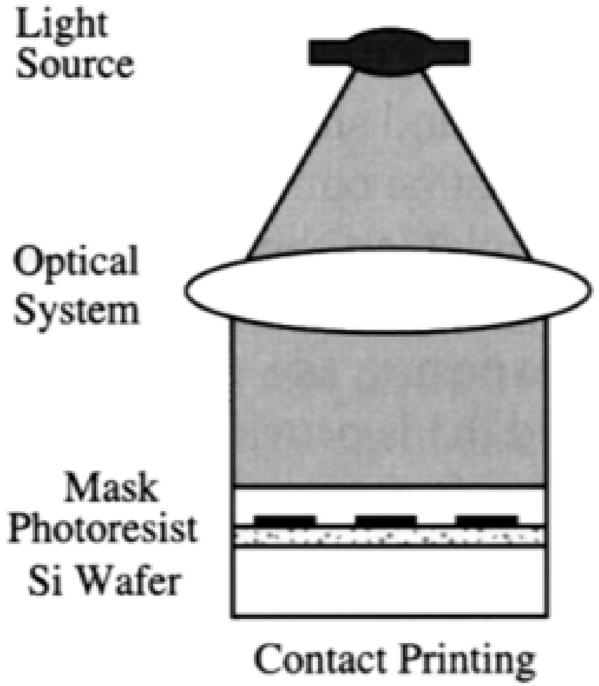
Printing Techniques

- Contact: Directly place mask on photoresist, 1:1 magnification
- Proximity: Slightly separate mask from photoresist, 1:1 magnification
- Projection: Use optics to project the mask pattern onto the resist, reduces the size of the image



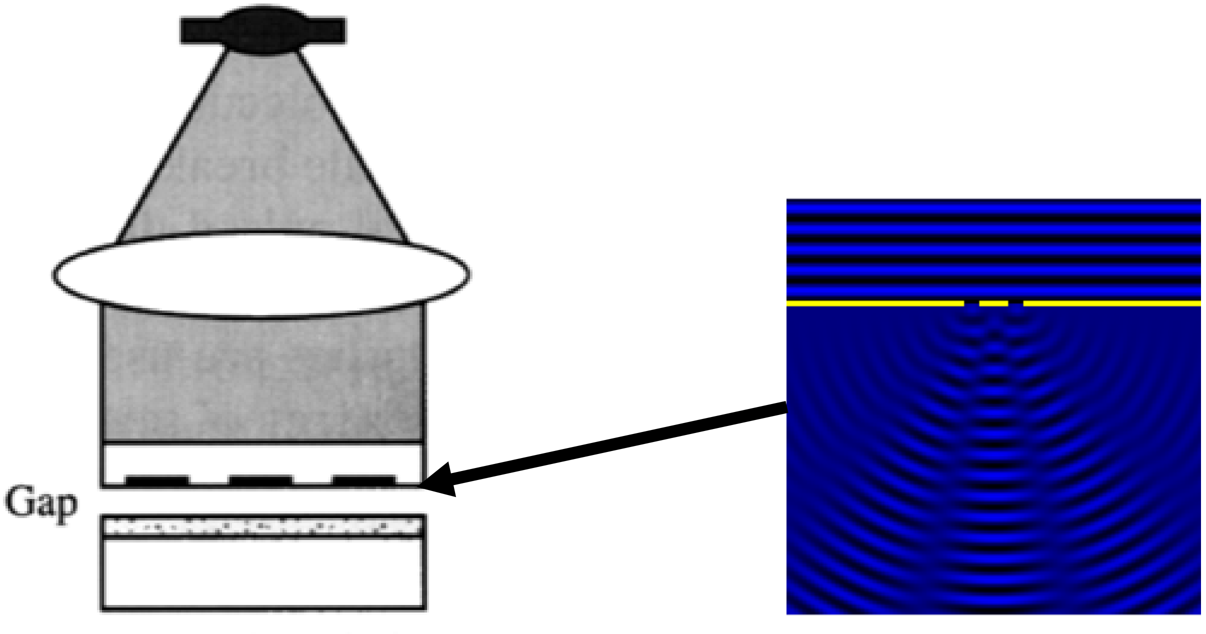
Contact Printing

- Resolution $< 0.5\ \mu m$
- Cheap
- But mask accumulates junk and gets damaged, limiting mask reusal



Proximity Printing

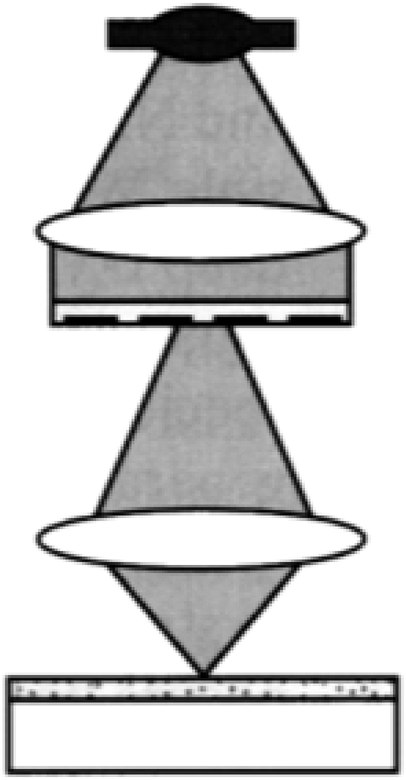
- Resolution $\sim \sqrt{\lambda g}$
  - λ: wavelength
  - g: gap (~tens of microns)
  - Limited by diffraction of light
- Mask damage reduced



Proximity Printing

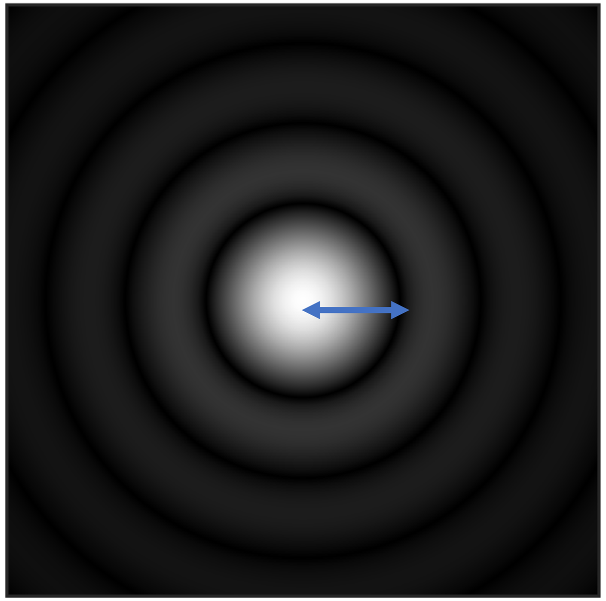
Projection Printing

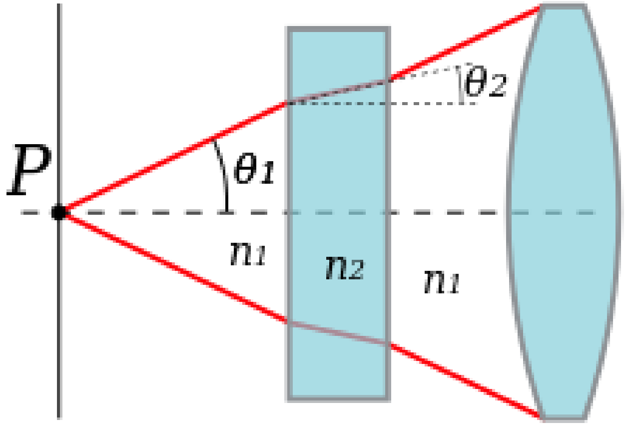
- Resolution can get to $\sim 0.2\ \mu m$ with UV light
- Expensive (the ASML EUV tool shown earlier is >$100M dollars!!!)



Projection Printing

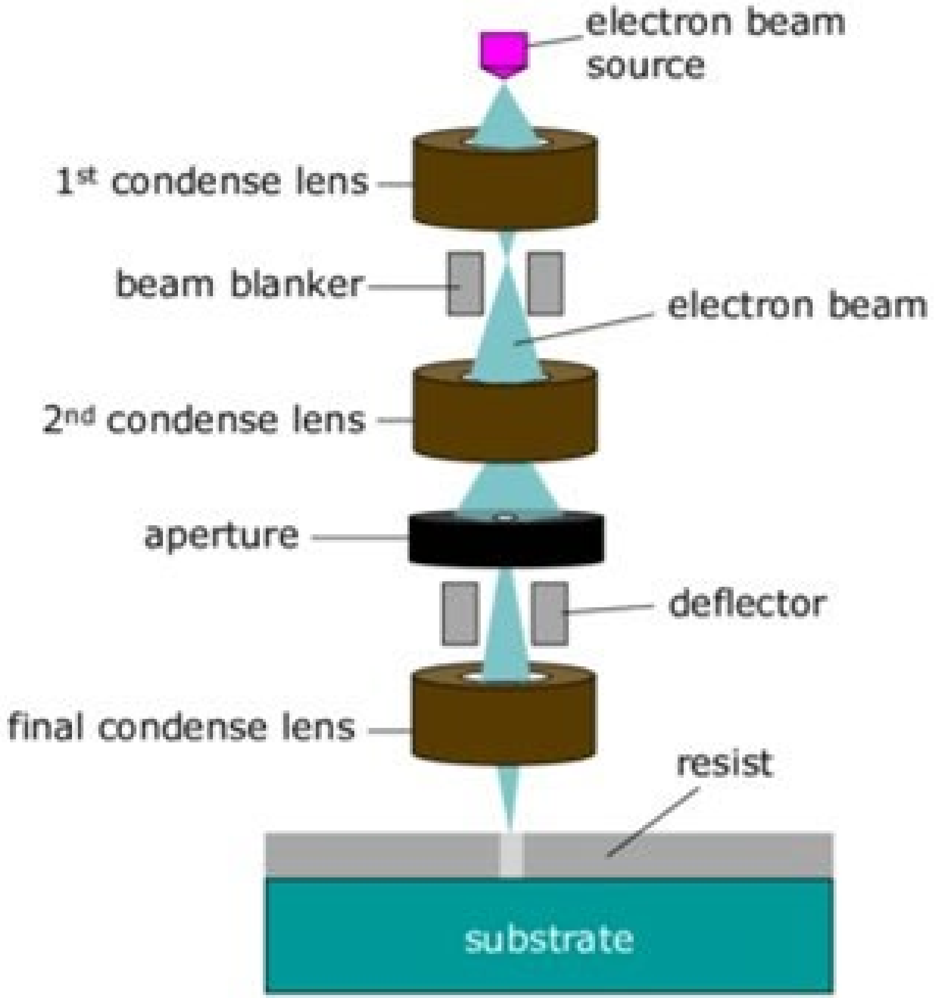
Resolution (Proximity Printing)





- Resolution: $R = k_1 \frac{\lambda}{NA}$
- $0.25 < k_1 < 1, NA = n \sin(\theta)$
- Numerical aperture *NA*: measure of the angles over which the system can accept light
- How to improve resolution?
  - Lower wavelength light: optics are hard!
  - Increase NA: increase the refractive index *n!* Use “immersion lithography” where a liquid is placed between the optics and the wafer.

Electron Beam (e-beam) Lithography

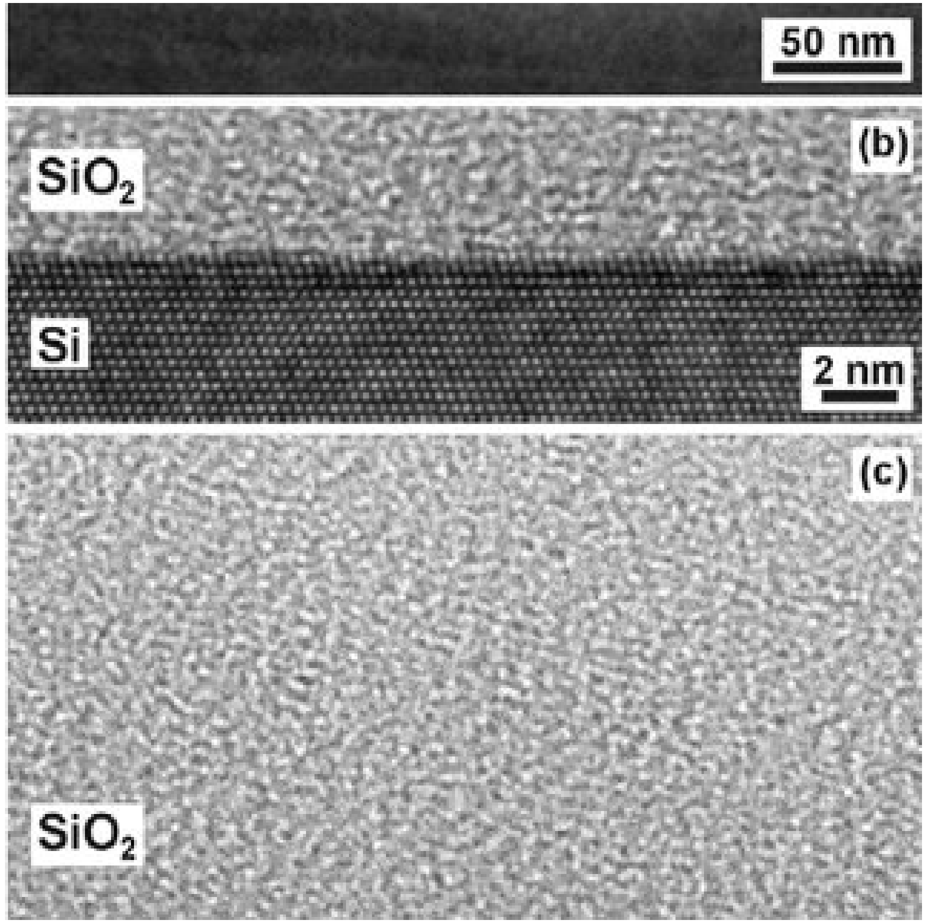


- Small electron wavelength: $\lambda = \frac{12.3}{\sqrt{V}}$
  - V is voltage applied (usually tens of kV)
- $NA{\sim}0.002 = 0.005$
- $R{\sim}1\ nm$
- But slow throughput ☹

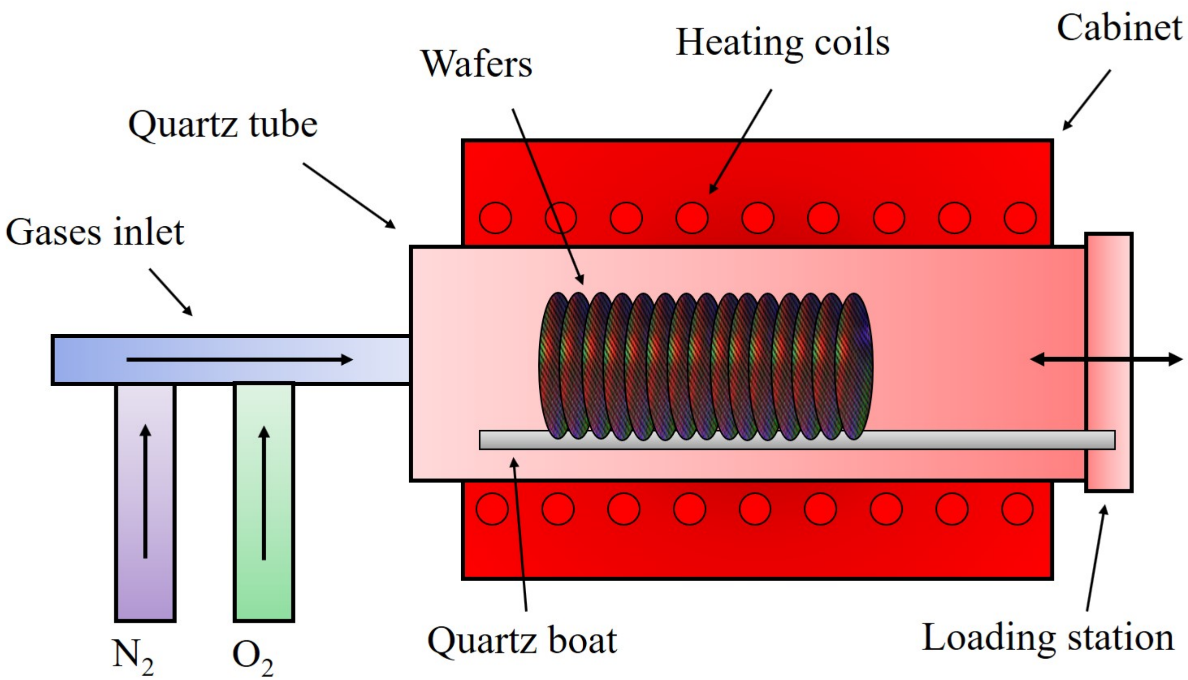
Thermal Oxidation

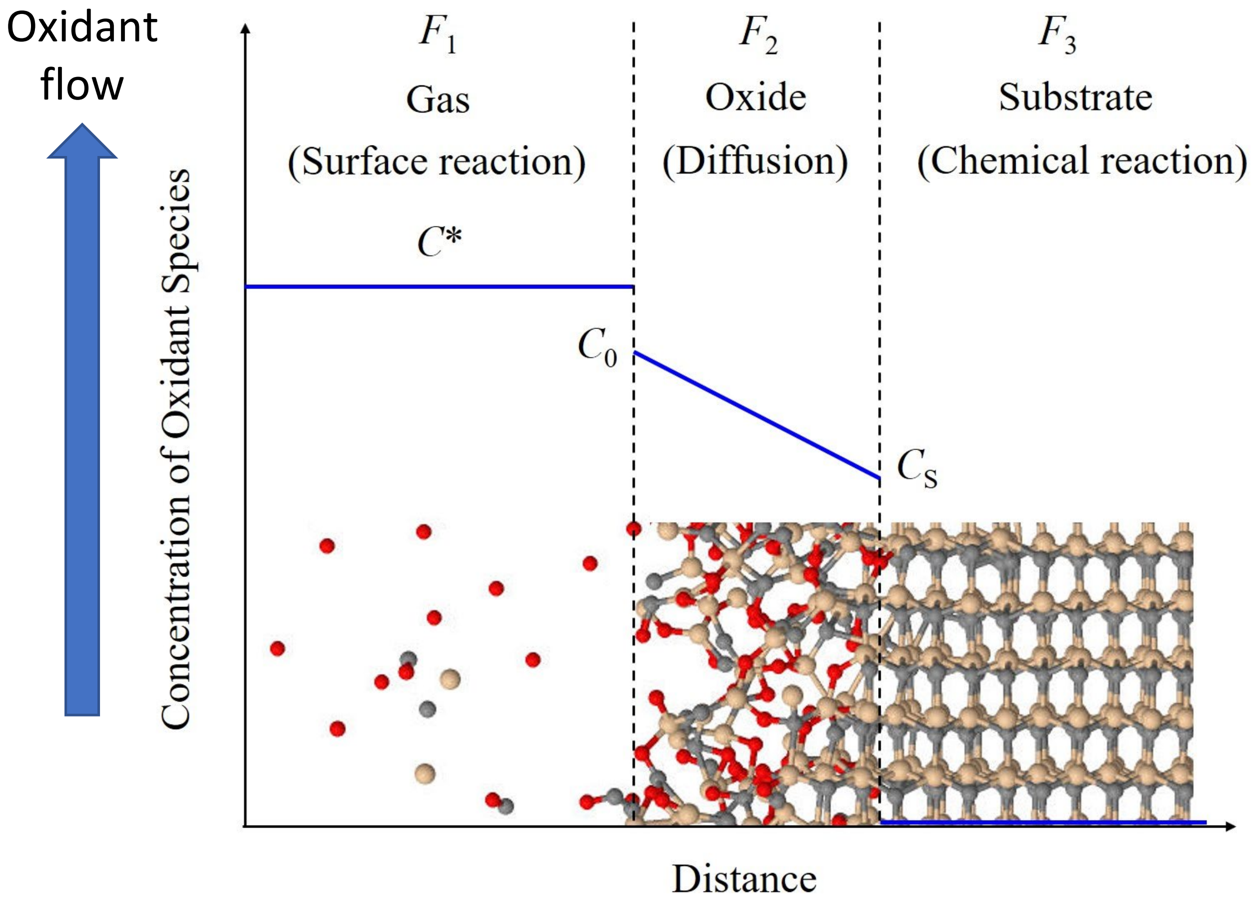
Why SiO_2?

- Native oxide on silicon (stable interface)
- Great insulator: $\rho > 10^{20}\,\Omega\,cm$
- High breakdown threshold: $E > 10\ MV/cm$
- Conformal growth on silicon
- Good diffusion/implant mask
- Good etching selectivity between Si and SiO_2 (to be discussed in the etching section!)



Thermal Oxidation Kinetics



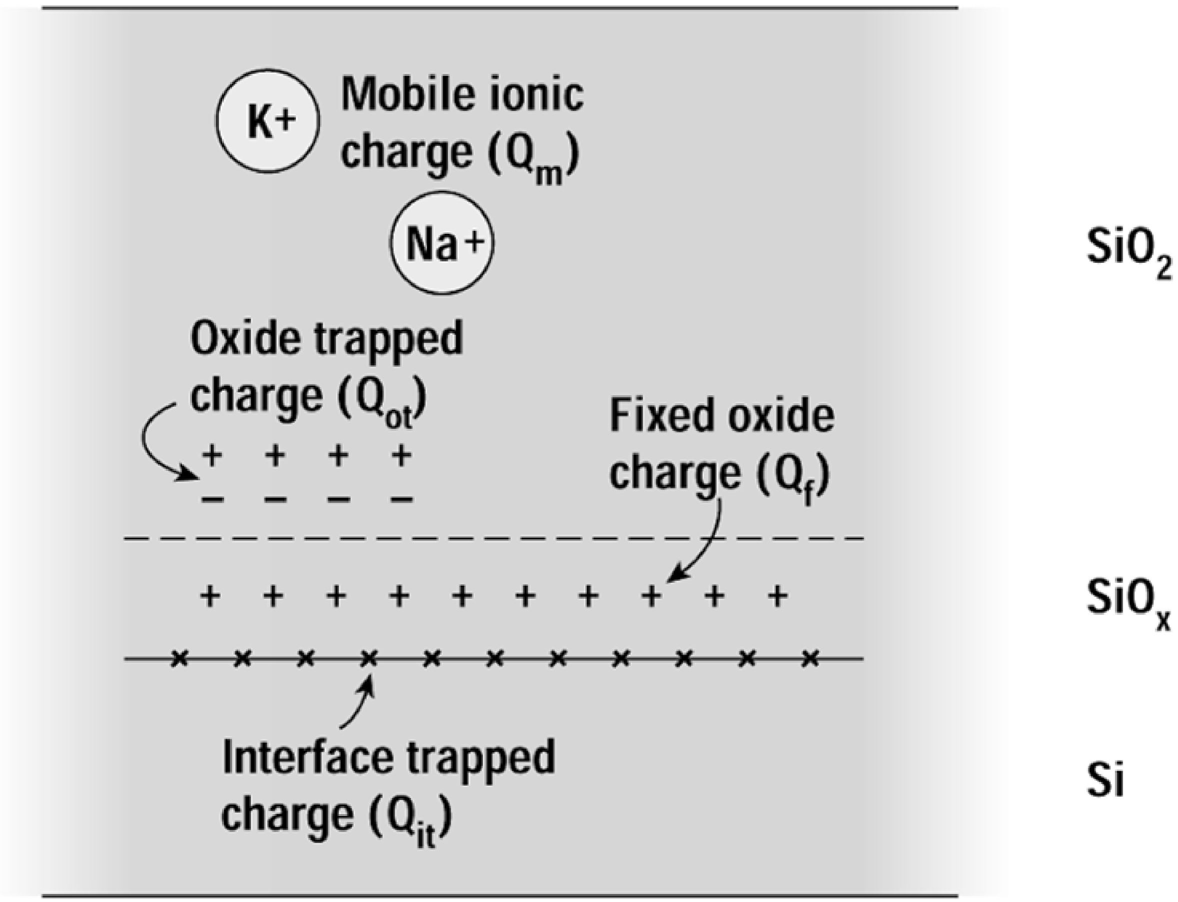


Wet and Dry Oxidation

- Dry: $Si + O_2 \rightarrow SiO_2$
  - Slow growth (~3 hours to grow 200 nm of oxide at 1100°C!)
  - Higher quality oxide, usually what is used for making electronic devices
- Wet: $Si + 2H_2O \rightarrow SiO_2 + 2H_2$
  - Fast growth (~3 hours to grow 1 um of oxide at 1100°C)
  - Lower quality than dry oxide (less dense, more dangling bonds), so usually used as a general “field” oxide to electrically isolate adjacent devices

Improving Oxide Quality

- Undesired charge leads to unexpected electronic characteristics
  - Metal contaminants → mobile ions
  - Fast growth → SiO_x instead of SiO_2
- Solutions:
  - Include some HCl in the gas to react with the mobile ions (e.g. $Na^+ + Cl^- \rightarrow NaCl$)
  - When cooling down, use inert gas (Argon or Nitrogen) so no added unwanted oxidation
  - Anneal at ~450°C at end in “forming gas” ($10\%H_2+90\%N_2$) so hydrogen passivates dangling bonds



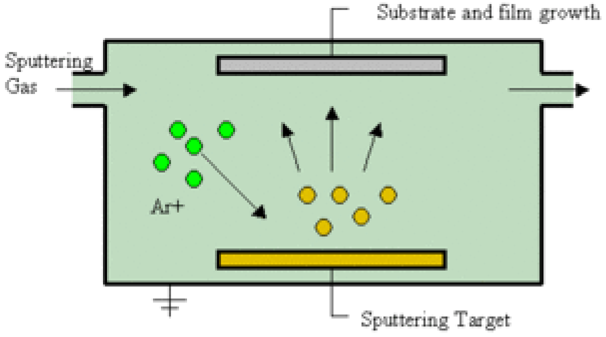
Thin Film Deposition

Chemical Vapor Deposition

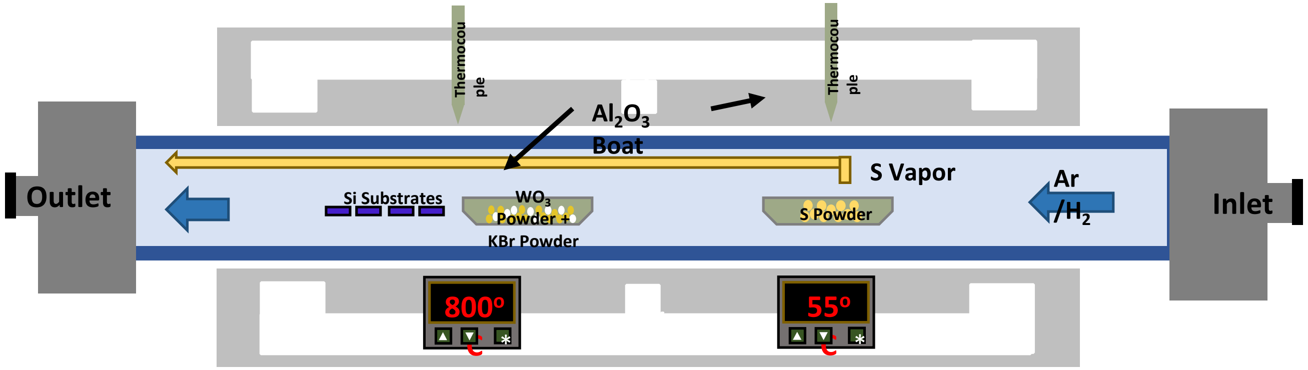
- Low Pressure CVD
- Plasma-enhanced CVD
- Atomic Layer Deposition

Physical Vapor Deposition

- Sputtering

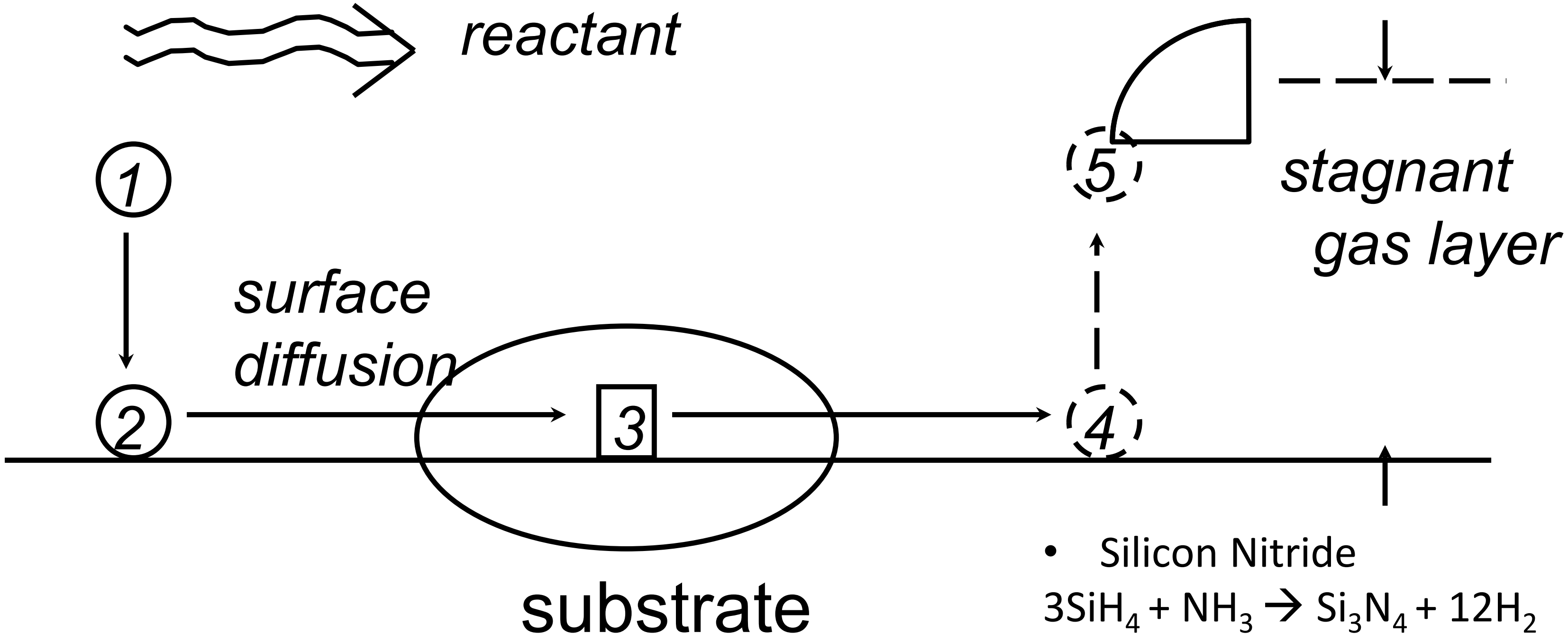


- Evaporation



Cho, J., et al. *Advanced Functional Materials* 30.6 (2020).

CVD Kinetics



1 = Diffusion of reactant to surface
2 = Absorption of reactant to surface
3 = Chemical reaction
4 = Desorption of gas by-products
5 = Outdiffusion of by-product gas

- Silicon Nitride

$3SiH_4 + NH_3 \rightarrow Si_3N_4 + 12H_2$

- Polysilicon

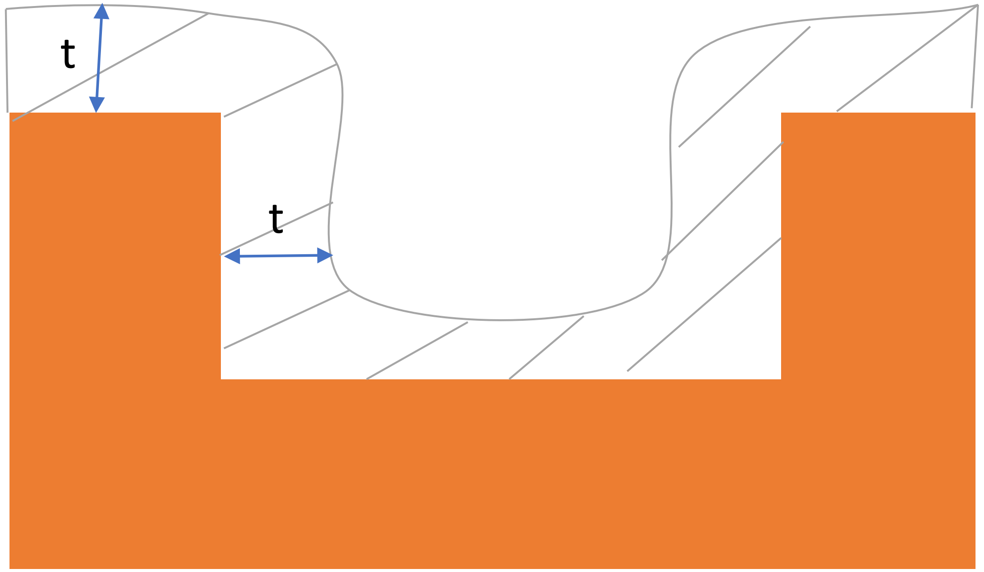
$SiH_4 \rightarrow Si + 2H_2$ (600 °C)

Note: deposition of single crystalline films generally requires "lattice-matched substrates" and high temperatures.

Based on EE143 slides from A. Javey

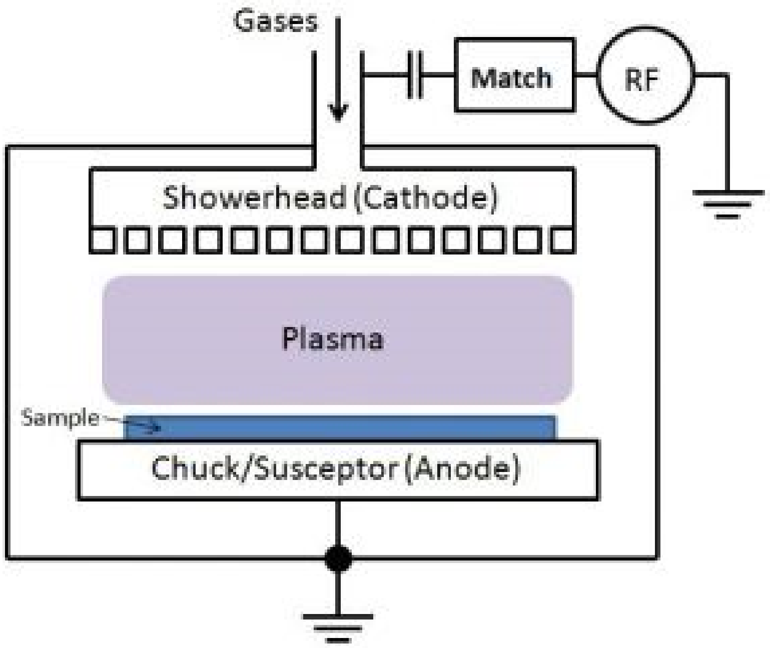
Low-Pressure Chemical Vapor Deposition (LPCVD)

- Pressure ~100 mTorr, Temperature ~700-900°C
  - Atmospheric pressure is 760 Torr
- Conformal deposition!
- Deposition rate: ~few nm/minute



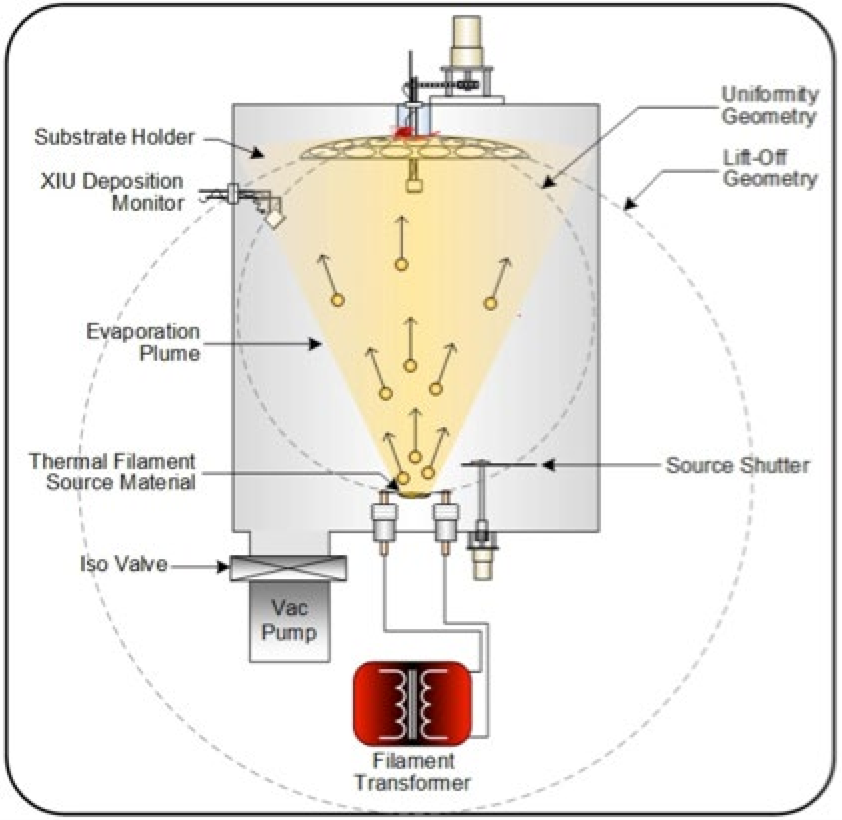
Plasma-Enhanced Chemical Vapor Deposition (PECVD)

- Temperature ~200-400°C
- Plasma (low pressure gas with ions + free electrons) provides extra energy to lower the process temperature!
- Deposition rate ~10-100 nm/minute
- Lower film quality

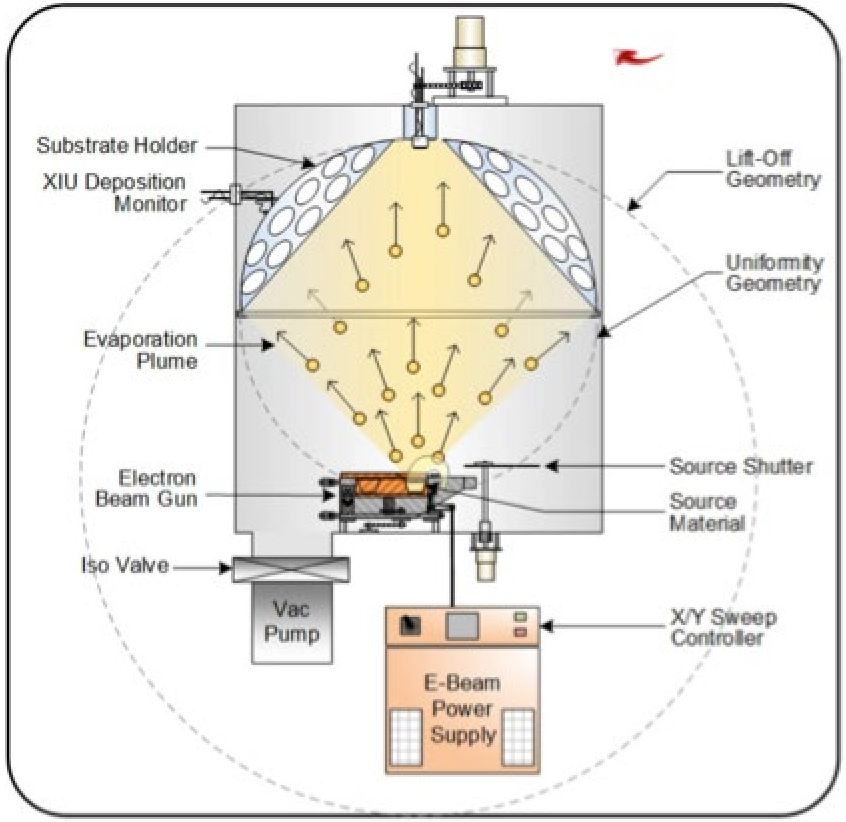


Physical Vapor Deposition—Evaporation

- Material is heated inside a vacuum chamber until it evaporates
- The molecules travel to the target substrate and form a film
- Pressure < 10^{-5} Torr



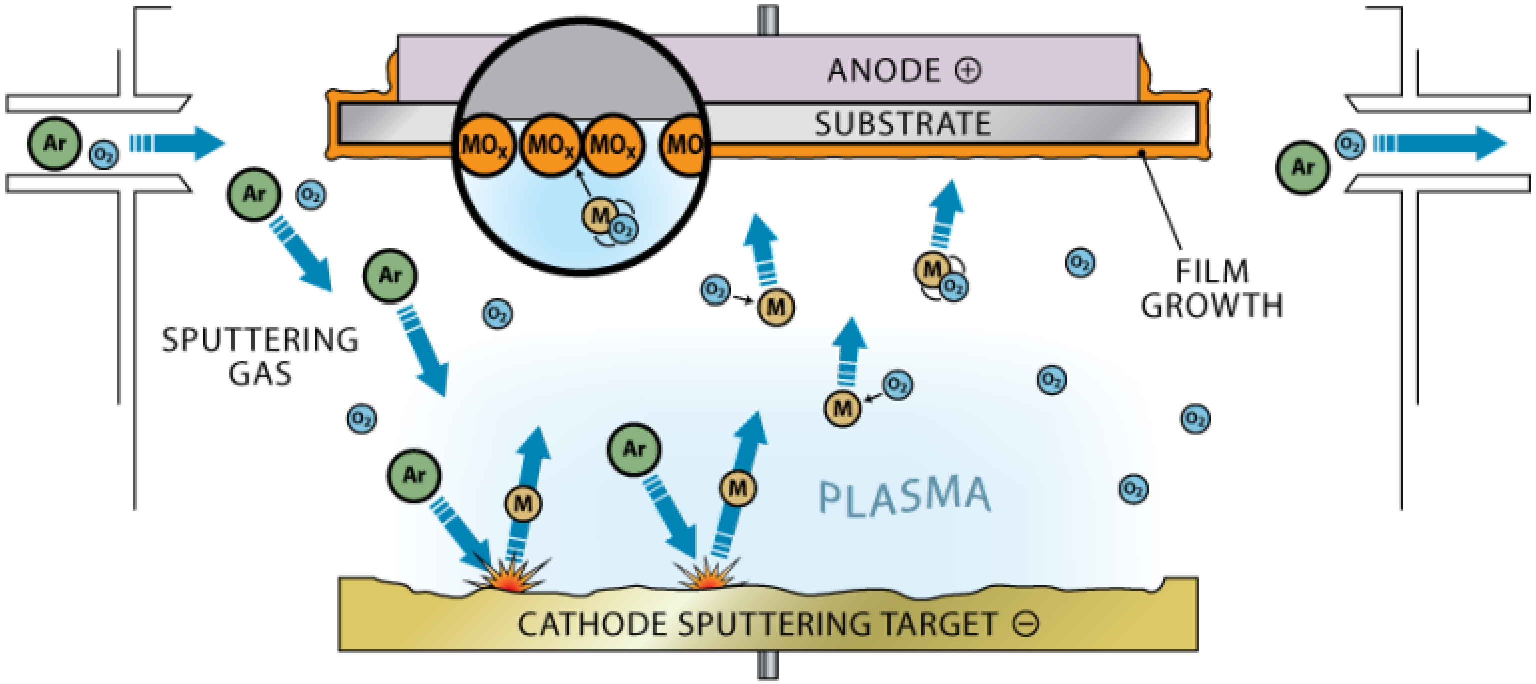
Thermal



E-beam

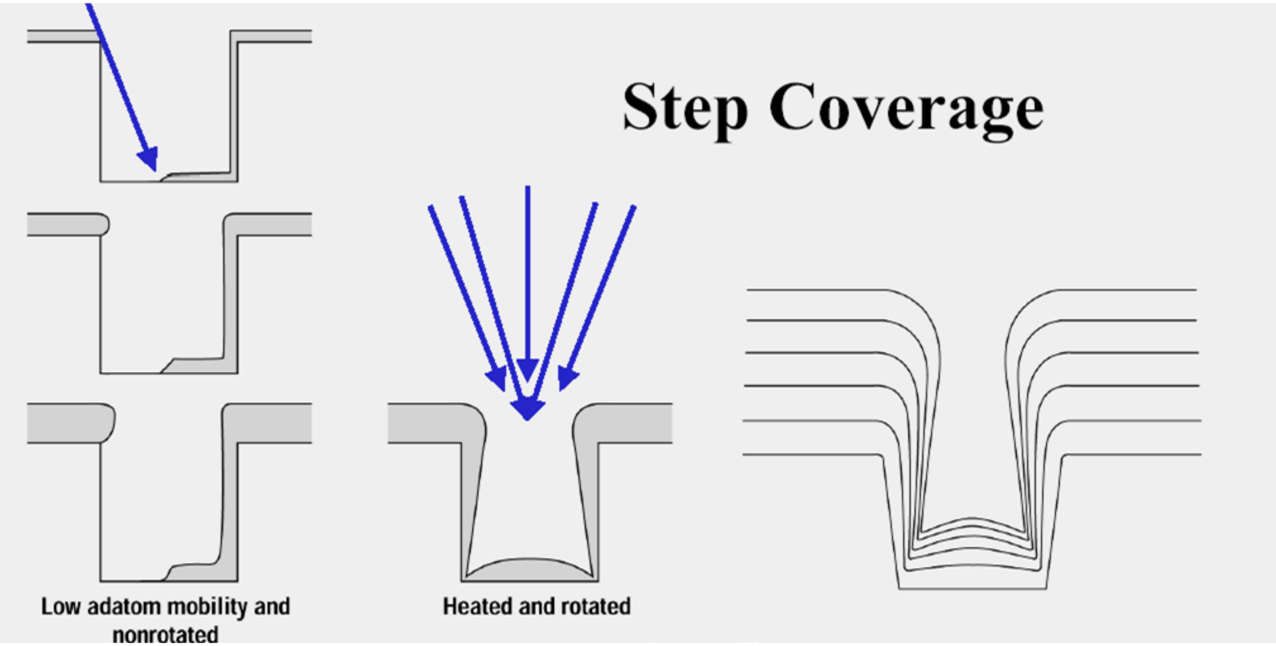
Physical Vapor Deposition—Sputtering

- Plasma (usually Argon) bombards a source, knocking off atoms which travel to the substrate and get deposited
- Pressure ~1-10 mTorr



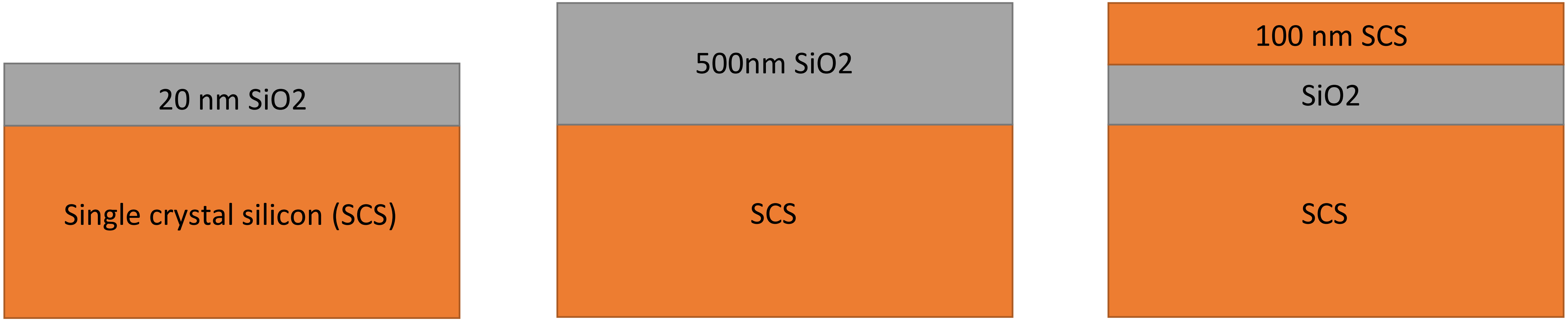
Physical Vapor Deposition—Summary

- Usually used for depositing metals, although some insulators and semiconductors can be deposited as well.
- Issue: step coverage ("line of sight" process)
  - Rotate the substrate ("planetary stage")
  - Heat the substrate
- In general, sputtering gives better control over the composition, and has better lateral thickness uniformity.
  - But the setup is quite complex.



First Process Integration Question!

How would you make these structures?



20 nm SiO2

Single crystal silicon (SCS)

500nm SiO2

SCS

100 nm SCS

SiO2

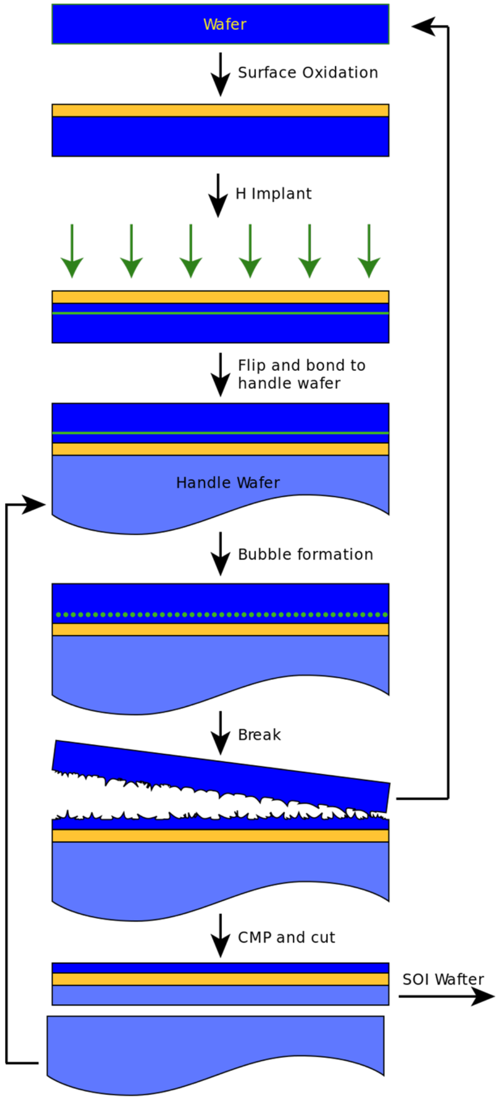
SCS

First Process Integration Question!

How would you make these structures?

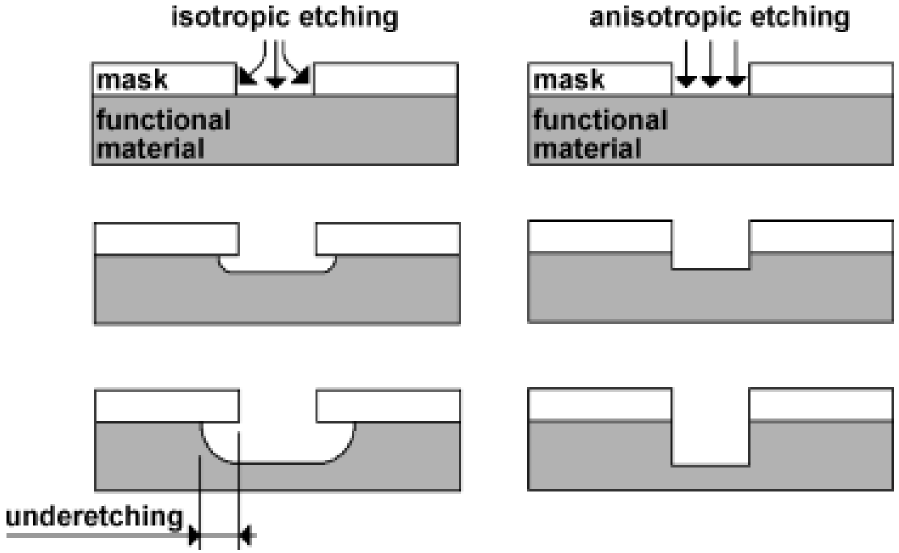
- 50 nm SiO_2: dry oxidation
- 500 nm SiO_2: wet oxidation
- Silicon on Insulator (SOI) wafer: “Smart Cut”

1. Start with 2 wafers
2. Thermal oxidation of wafer 1
3. Ion implant hydrogen below the thermal oxide
4. “Wafer bonding”: flip wafer 1 and place on wafer 2. Anneal to bond the wafers together.
5. “Bubble formation”: low temperature anneal causes hydrogen gas bubbles, weakening the layer
6. Split the wafers and polish the rough surface.

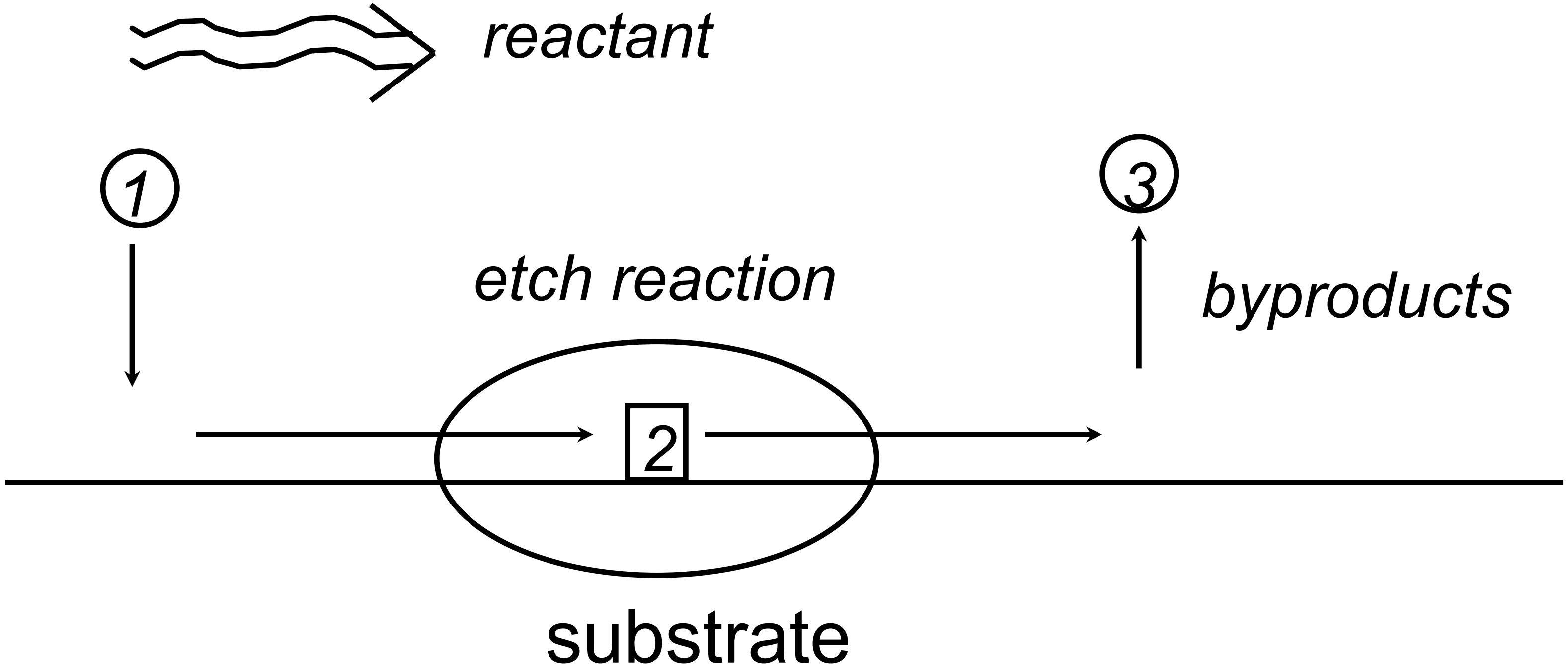


Etching Figures of Merit

- Etch Rate
- Uniformity
- Selectivity
  - How well does the method etch material 1 while not etching material 2?
- Anistropy
  - Does the method etch in all directions, or only in one direction, or somewhere in between?



Wet Etching Kinetics



- Wet etching usually done with an acid
- Etch rate determined by temperature, concentration and the material/chemical choice

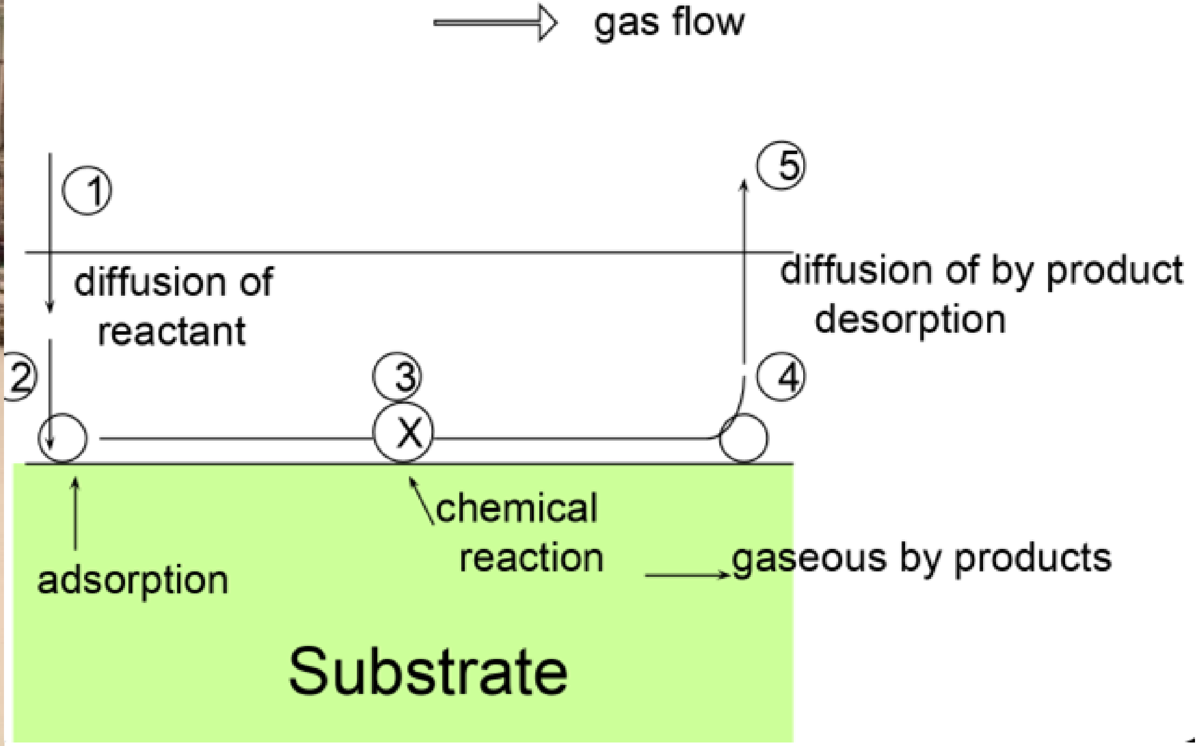
Wet Etching Summary

- Examples:
  - $SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$
  - Aluminum etchant: phosphoric acid (etch aluminum oxide) + acetic acid + nitric acid (oxidant) + water (at ~30°C)
- Pros:
  - High selective, e.g. HF and SiO_2 vs Si
  - Straightforward
- Cons:
  - Isotropic*
  - Hard to control exactly
  - Particulate contamination

Reactive Ion Etching (RIE)

Enhance chemical reaction!

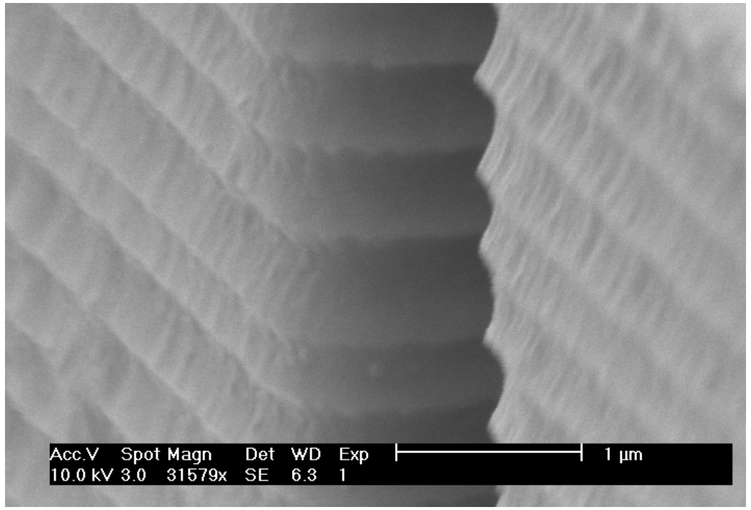
Plasma generates (1) ions **(2) Activated neutrals**

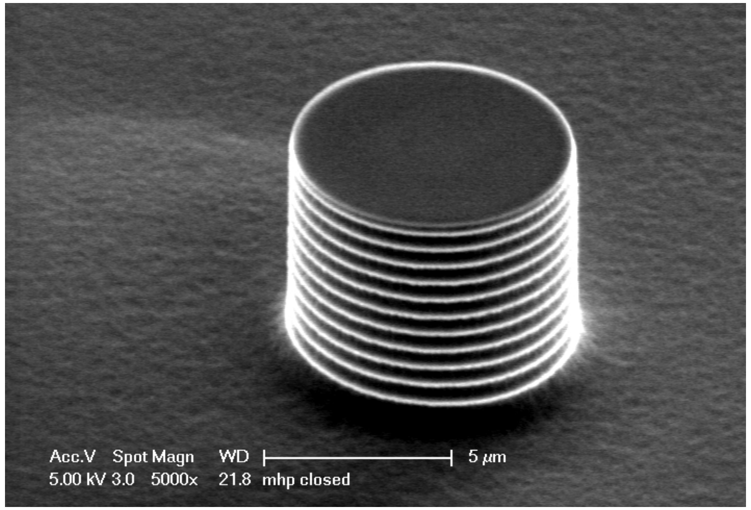


Based on EE143 slides from A. Javey

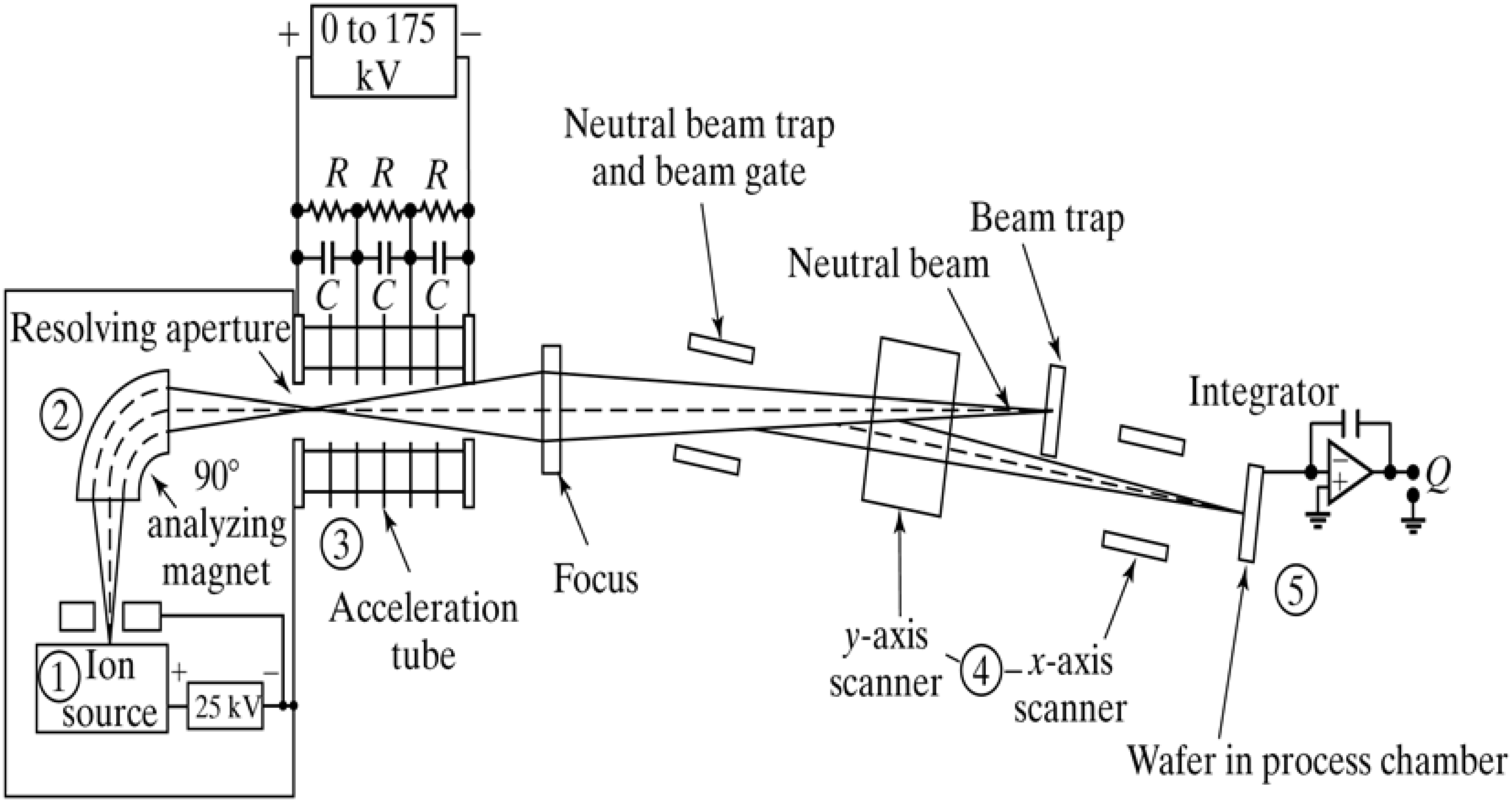
Deep Reactive Ion Etching (DRIE)

- Similar to RIE, but special gas chemistry forms a polymer (“sidewall inhibitor”) on the sidewalls as the trench is being etched
- This protective polymer prevents undercutting, enabling the formation of very deep and narrow structures
  - Dry etching is generally anisotropic!





Ion Implantation

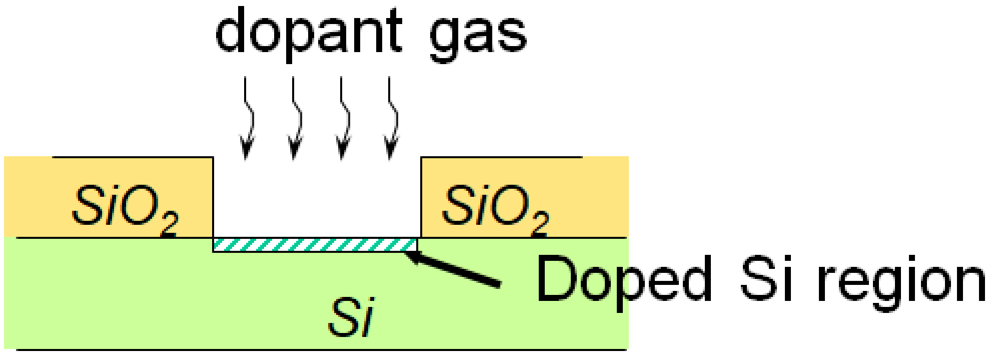


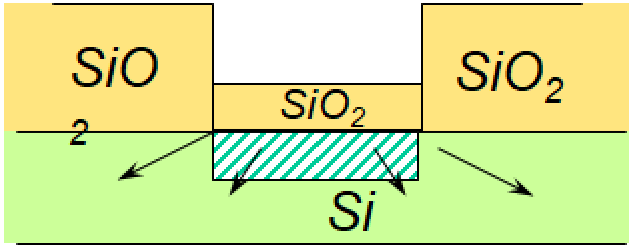
- Ions are accelerated into the target wafer
- Because of material damage, need to anneal afterward to "heal" the wafer and let defects move into place
- Pros:
  - Can implant almost anything
  - Precise dose and depth control
  - Room temperature process
- Cons:
  - Expensive

Diffusion Doping

(1) Pre-deposition

(2) Drive-in

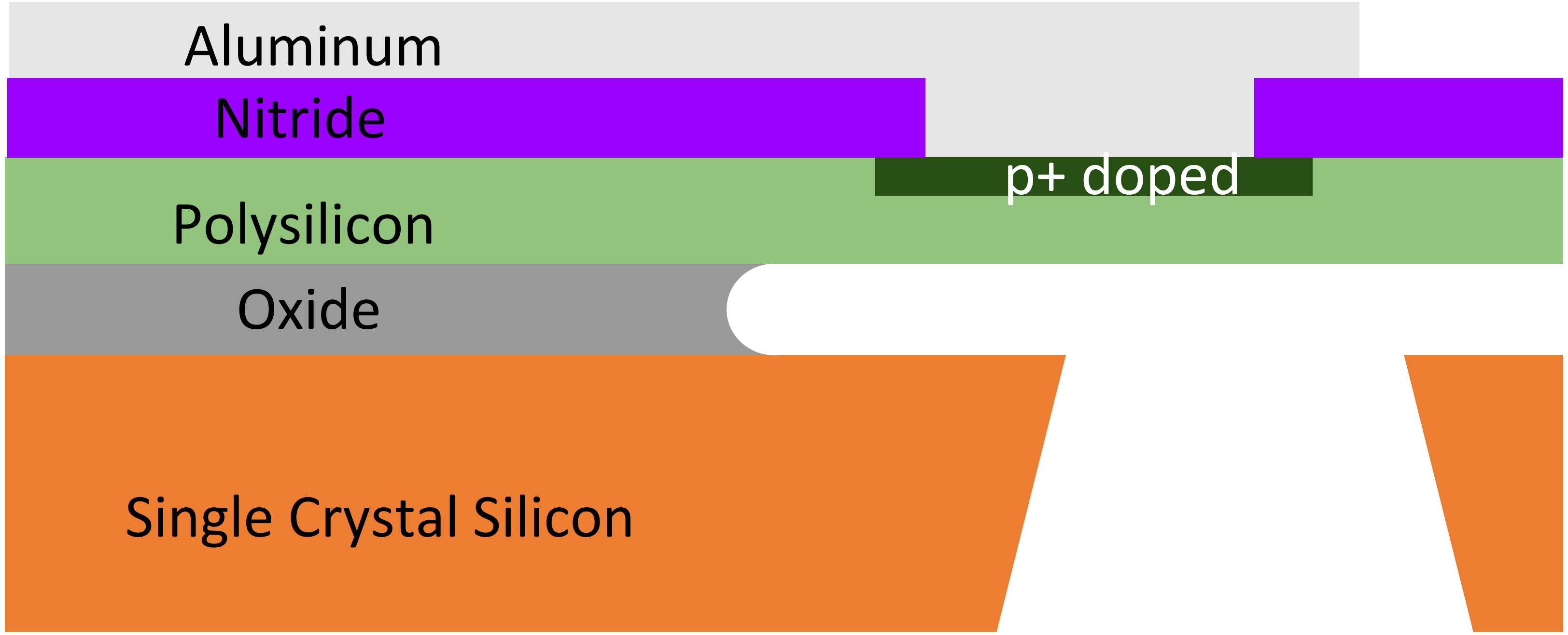




Based on EE143 slides from A. Javey

Second Process Integration Question!

How would you make this structure?

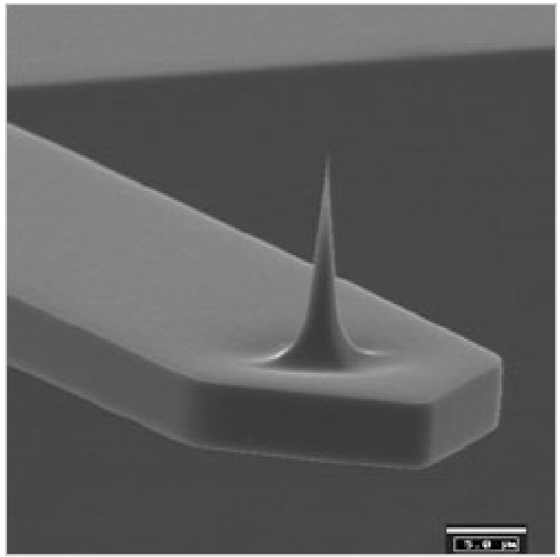


Based on EE143 slides from A. Javey

Second Process Integration Question!

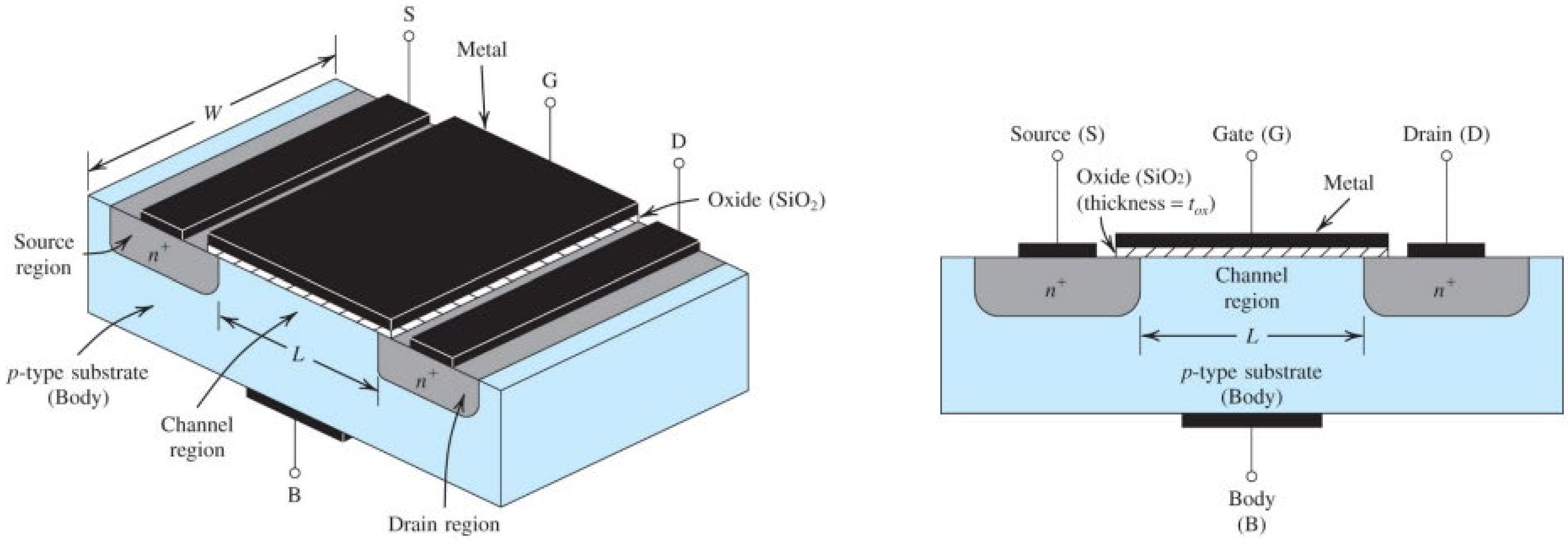
How would you make this structure?

1. Oxidation
2. Polysilicon CVD
3. Ion implant, e.g. boron
    a. deposit ion implant mask, e.g. a photoresist
    b. photolithography to open up hole
    c. implant
    d. anneal
4. Silicon Nitride CVD
5. Photolithography and RIE etch nitride to open hole
6. Sputter Aluminum
7. Photolithography and etch Aluminum
8. Photolithography and etch nitride and poly
9. **Flip the wafer. Wet oxidation of the back.**
10. RIE down to open up the hole.



AFM cantilever made with similar backside processing

MOSFET Transistors

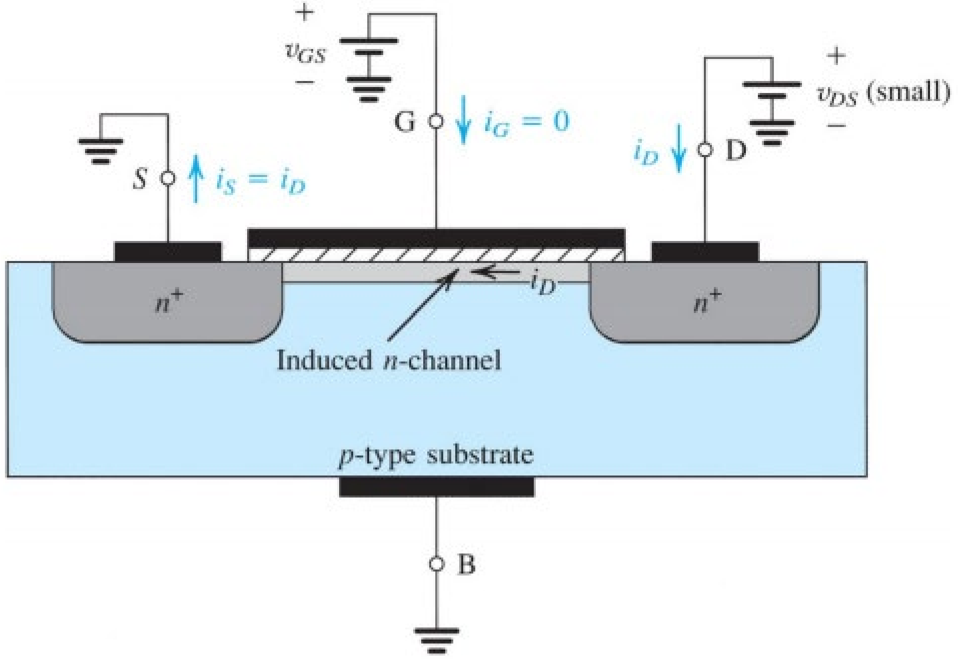


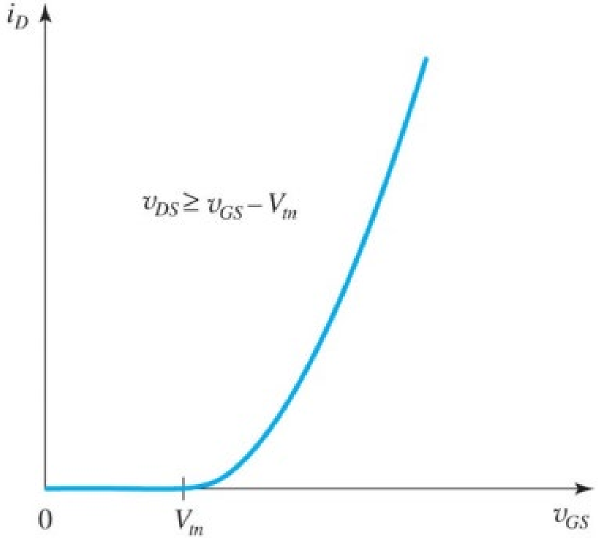
(a)

(b)

MOSFET as a Switch

- Diagram to the right is that of a “NMOS”: when turned “on”, the current is carried by electrons
- A “PMOS” would be the opposite: current carried by holes
- When the gate voltage applied is higher than some threshold voltage, “inversion” in the channel occurs and current can flow!

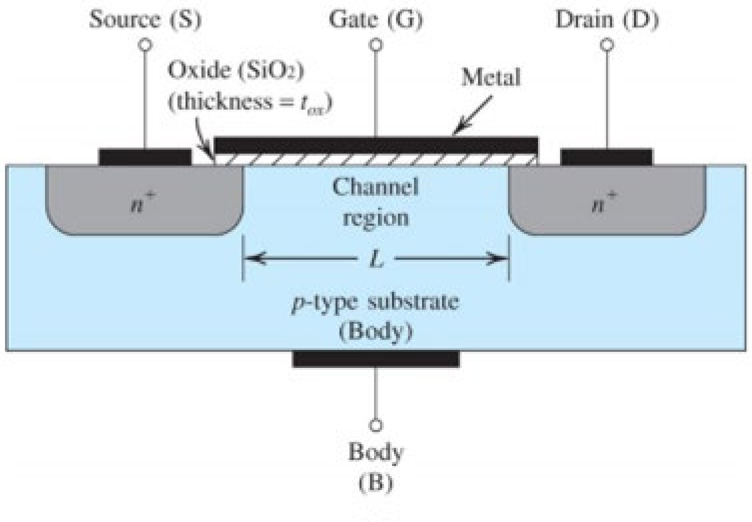




Third Process Integration Question!

How would you make a simple **PMOS**?

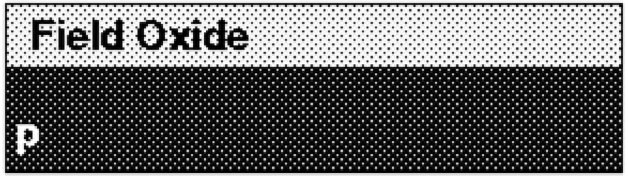
For reference, here is a picture of the **NMOS** from earlier (ignore the body electrode)



(b)

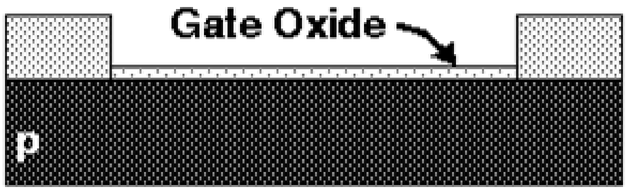
Example Process Flow Revisited

Week 2: Field Oxidation - 5200 A

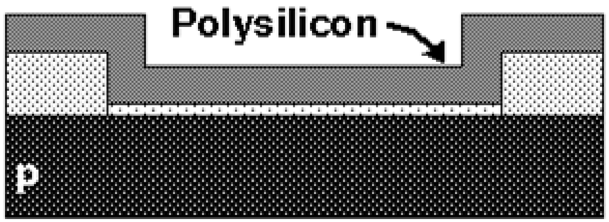


Week 3: Active Area Photolithography

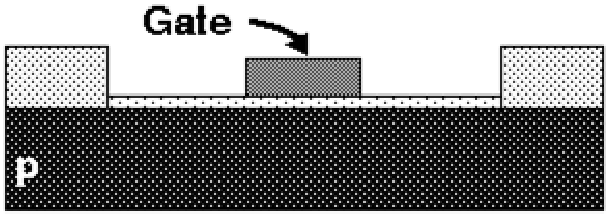
Week 4: Gate Oxidation - 800 A



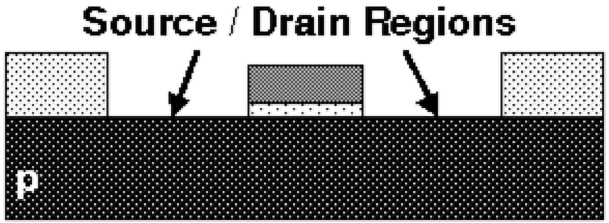
Week 5: Poly-Si Deposition



Week 6: Gate Photolithography



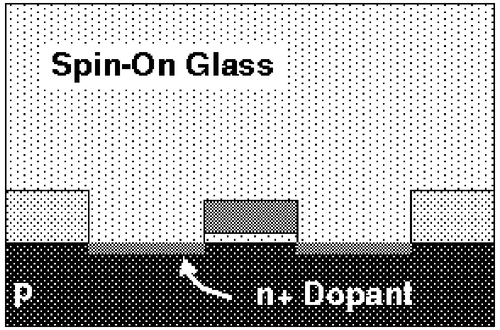
Week 6: Clear Source and Drain



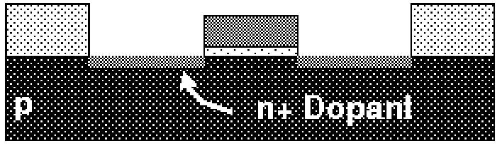
Based on EE143 slides from A. Javey

Example Process Flow Revisted (cont.)

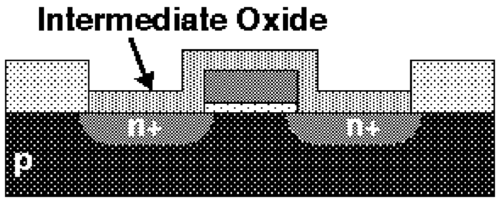
Week 7a: Source-Drain Deposition (N+)



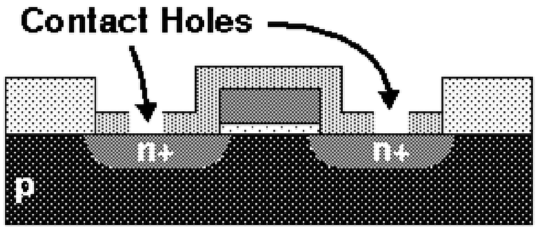
Week 7b: Spin-on Glass Strip



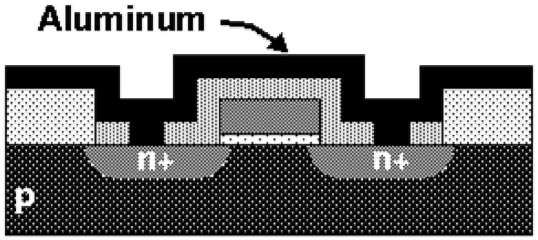
Week 7b: Drive-In Oxidation



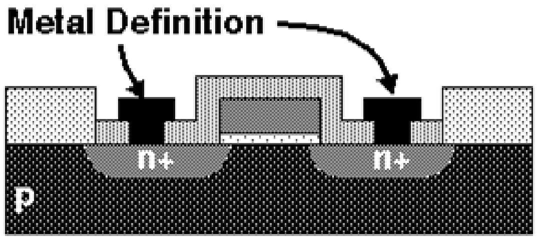
Week 8: Contact-Hole Cut (Mask #3 - CONT)



Week 9: Metallization



Week 10: Metal Definition



Based on EE143 slides from A. Javey

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Thank you for listening!

Joy Cho, Matt Yeh – Saturday, November 14th, 2020

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